2207/304
DIGITAL PRINCIPLES
AND MICROPROCESSORS
June/July 2018
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING (AVIONICS) (COMMUNICATION AND NAVIGATION OPTION)

DIGITAL PRINCIPLES AND MICROPROCESSORS

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:
Instruction Set (Intel 8080/8085);
Non-programmable scientific calculator.
*Answer any **FIVE** of the **EIGHT** questions in the answer booklet provided.*
All questions carry equal marks.
Maximum marks for each part of a question are as shown.
Candidates should answer the questions in English.

This paper consists of 8 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

1. (a) Convert the binary number $101111 \cdot 0101$ into:

(i) octal;

(ii) hexadecimal;

(iii) decimal.

(6 marks)

(b) Evaluate each of the following in the given bases:

(i) $(72)_8 \times (3)_8$;

(ii) $(110110)_2 \times (101)_2$;

(iii) $(11101100)_2 \div (10)_2$.

(9 marks)

(c) Convert the 8-4-2-1 BCD number 10010111 0110 into:

(i) decimal;

(ii) excess - 3;

(iii) binary.

(5 marks)

2. (a) (i) Define each of the following with respect to digital logic:

(I) literal;

(II) canonical.

(2 marks)

(ii) Simplify each of the following using Boolean Algebra.

(I) $Z_1 = w.x + w.\bar{x}.y$

(II) $Z_2 = \overline{(x+y).(\bar{x}+\bar{y})}$

(III) $Z_3 = xy + w.\bar{y} + w.y + xyv$

(6 marks)

(b) Figure 1 shows a DTL NAND gate. When $V_{BE(sat)} = 0.8\ V$ the output $y = 0.5\ V$ and $V_{CE(sat)} = 0.2\ V$. The voltage drop across a forward conducting diode is 0.7 V. The inputs of the gate are obtained from the outputs of a similar gate.

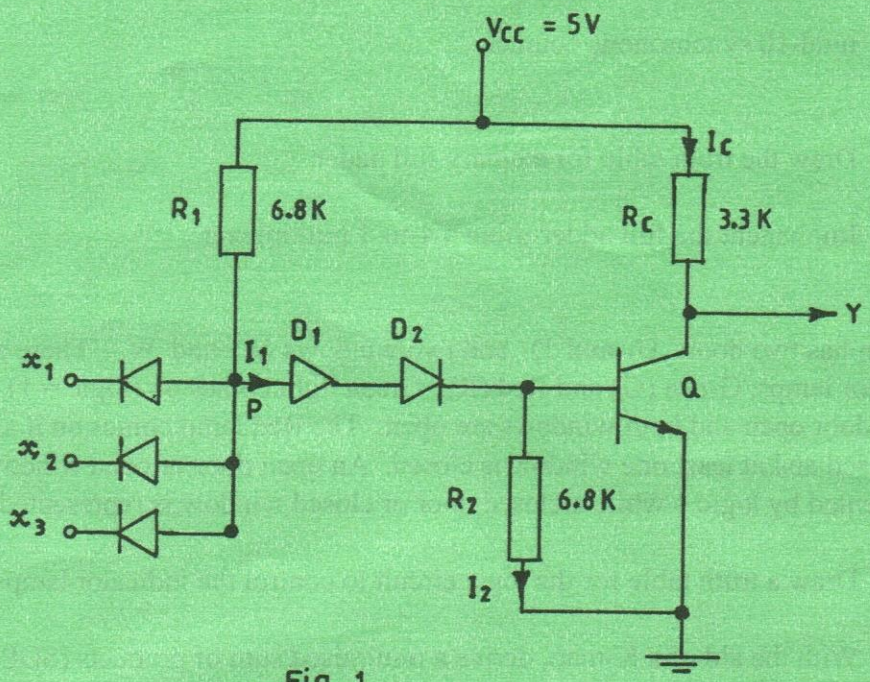

Fig. 1

Determine the:

(i) current gain ($h_{FE(min)}$) for the transistor; (7 marks)

(ii) average output power of Q. (5 marks)

3. (a) For a positive-edge triggered J-K/Flip-flop:

(i) sketch its symbol;

(ii) draw its truth table.

(6 marks)

(b) (i) Draw a counting sequence (state) diagram for an asynchronous modulo - 5 down counter.

(ii) Implement the counter in b(i) using JK-FF.

(6 marks)

(c) (i) Using D flip-flops, draw a schematic block diagram of a 4-bit parallel-in parallel-out shift register.

(ii) State **one** application of the register in c(i).

(4 marks)

(d) The propagation delay of a flip-flop is 40 nS and that of a NAND gate is 15 nS. Determine the maximum clocking frequency for:

(i) mod-10 asynchronous counter;

(ii) mod-10 synchronous counter.

(4 marks)

4. (a) (i) Draw the truth table for a binary full adder.

(ii) Implement the full adder using a 4-to-1 multiplexer.

(8 marks)

(b) A room has two doors D_1 and D_2 and two windows W_1 and W_2. There are two indicator lamps, Green (G) and Red (R). Green light comes on (logic = 1) if at least one is door open and both windows are open. The Red lamp comes on if all doors are closed and at least one window is closed. An open door or open window is represented by logic 1 while a closed door or closed window is represented by logic O.

(i) Draw a truth table for the logic circuit to control the indicator lamps. (4 marks)

(ii) With the aid of a K-map, derive a minimised sum of products (SOP) logic expression for controlling the Green lamp, G. (4 marks)

(iii) draw a logic circuit diagram for controlling the green lamp (G) using NAND gates only. (4 marks)

5. (a) Differentiate between synchronous and asynchronous counters stating **one** merit for each. (4 marks)

(b) Figure 2 shows a logic diagram of a sequence generator.

(i) Derive the truth table showing the outputs Q_1, Q_2, Q_3, Q_4 after ten o'clock transitions. (4 marks)

(ii) Deduce the sequence of the generator from the output of the flip-flops. (2 marks)

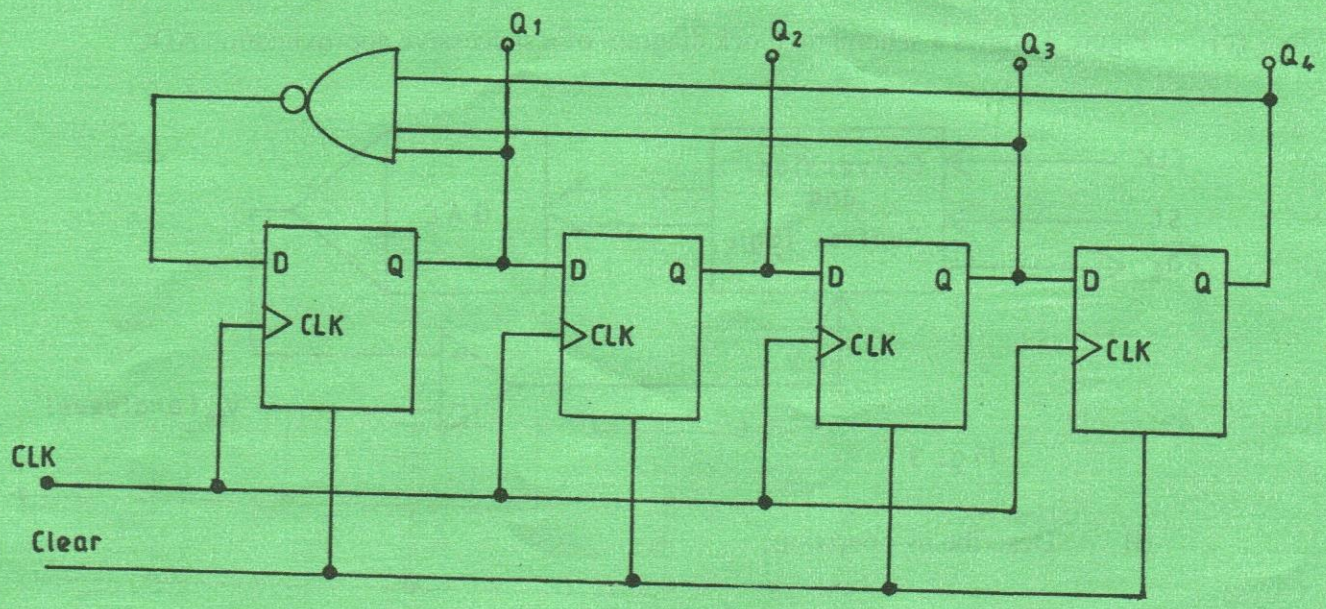

Fig. 2

(c) (i) Draw a schematic block diagram of a 3-bit ring counter using D-flip flops. (4 marks)

(ii) Describe the operation of the counter in (c)(i). (4 marks)

(iii) State **one** merit and **one** demerit of the ring counter. (2 marks)

6. (a) Define each of the following with respect to digital-to analogue converters (ADCs):

(i) monotonicity;

(ii) dynamic range.

(2 marks)

(b) A 16-bit digital-to-analogue converter (DAC) has a 10-V reference voltage. Compute each of the following for the DAC:

(i) resolution, in volts:

(ii) analogue output for a binary input of $(0001\ 1100\ 1100\ 0100)_2$. (6 marks)

(c) Figure 3 shows a schematic block diagram of a successive approximation ADC.

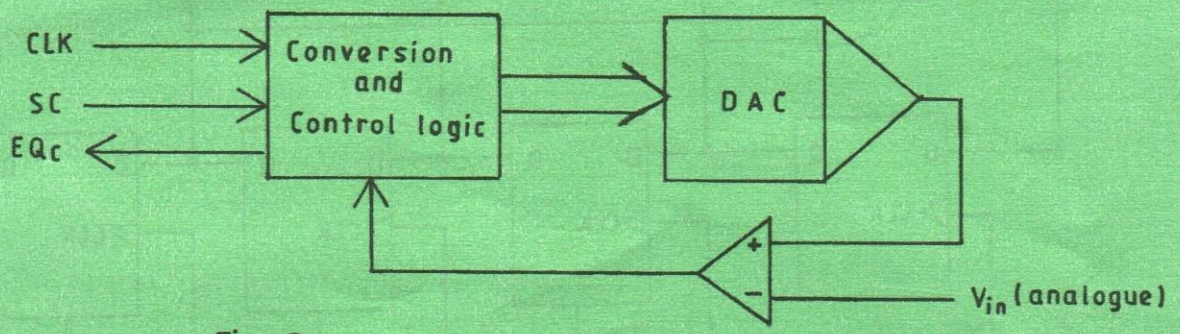

Fig. 3

(i) Describe its operation;

(ii) State **one** merit and **one** demerit of the ADC.

(7 marks)

(d) State:

(i) **three** functions of a computer interface;

(ii) **two** merits of direct memory access (DMA).

(5 marks)

7. (a) Table 1 shows an Intel 8085 program segment.

Table 1

LXI H, 2030 H
STA 4090 H
DAD B
INX H

Determine the:

(i) addressing mode of each instruction;

(ii) length of each machine code instruction in bytes.

(4 marks)

(b) With the aid of a flowchart, write an assembly language programme to generate a saw tooth waveform. The waveform will be output to a Digital Analogue Converter (DAC) at port address FE H. (10 marks)

(c) Explain the functions of any **three** microprocessor registers. (6 marks)

8. (a) Outline the logical steps for testing faults in a microprocessor-based system. (7 marks)

(b) Outline the procedure for testing a suspect open-circuit fault in resistor using a multimeter. (4 marks)

(c) (i) Define each of the following with respect to memory devices:

(I) word size;
(II) access time;
(III) non-volatile.

(ii) A semiconductor RAM chip is specified as 32K X 16. Determine the:

(I) number of address lines;
(II) number of data lines;
(III) memory capacity, in kilobytes.

(9 marks)

Instruction set of

8080/8085

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	28	DCX H	56	MOV D,M	81	ADD C	AC	XRA H	D7	RST 2
01	LXI B,D16	2C	INR L	57	MOV D,A	82	ADD D	AD	XRA L	D8	RC
02	STAX B	2D	DCR L	58	MOV E,B	83	ADD E	AE	XRA M	D9	–
03	INX B	2E	MVI L,D8	59	MOV E,C	84	ADD H	AF	XRA A	DA	JC Adr
04	INR B	2F	CMA	5A	MOV E,D	85	ADD L	B0	ORA B	DB	IN D8
05	DCR B	30	SIM	5B	MOV E,E	86	ADD M	B1	ORA C	DC	CC Adr
06	MVI B,D8	31	LXI SPD16	5C	MOV E,H	87	ADD A	B2	ORA D	DD	–
07	RLC	32	STA Adr	5D	MOV E,L	88	ADC B	B3	ORA E	DE	SBI D8
08	–	33	INX SP	5E	MOV E,M	89	ADC C	B4	ORA H	DF	RST 3
09	DAD B	34	INR M	5F	MOV E,A	8A	ADC D	B5	ORA L	E0	RPO
0A	LDAX B	35	DCR M	60	MOV H,B	8B	ADC E	B6	ORA M	E1	POP H
0B	DCX B	36	MVI M,D8	61	MOV H,C	8C	ADC H	B7	ORA A	E2	JPO Adr
0C	INR C	37	STC	62	MOV H,D	8D	ADC L	B8	CMP B	E3	XTHL
0D	DCR C	38	– –	63	MOV H,E	8E	ADC M	B9	CMP C	E4	CPO Adr
0E	MVI C,D8	39	DAD SP	64	MOV H,H	8F	ADC A	BA	CMP D	E5	PUSH H
0F	RRC	3A	LDA Adr	65	MOV H,L	8G	SUB B	BB	CMP E	E6	ANI D8
10	– –	3B	DCX SP	66	MOV H,M	91	SUB C	BC	CMP H	E7	RST 4
11	LXI D,D16	3C	INR A	67	MOV H,A	92	SUB D	BD	CMP L	E8	RPE
12	STAX D	3D	DCR A	68	MOV L,B	93	SUB E	BE	CMP M	E9	PCHL
13	INX D	3E	MVI A,D8	69	MOV L,C	94	SUB H	BF	CMP A	EA	JPE Adr
14	INR D	3F	CMC	6A	MOV L,D	95	SUB L	C0	RNZ	E8	XCHG
15	DCR D	40	MOV B,B	6B	MOV L,E	96	SUB M	C1	POP B	EC	CPE Adr
16	MVI D,D8	41	MOV B,C	6C	MOV L,H	97	SUB A	C2	JNZ Adr	ED	–
17	RAL	42	MOV B,D	6D	MOV L,L	98	SBB B	C3	JMP Adr	EE	ERI D8
18	– –	43	MOV B,E	6E	MOV L,M	99	SBB C	C4	CNZ Adr	EF	RST 5
19	DAD D	44	MOV B,H	6F	MOV L,A	9A	SBB D	C5	PUSH B	F0	RP
1A	LDAX D	45	MOV B,L	70	MOV M,B	9B	SBB E	C6	ADI D8	F1	POP PSW
1B	DCX D	46	MOV B,M	71	MOV M,C	9C	SBB H	C7	RST 0	F2	JP Adr
1C	INR E	47	MOV B,A	72	MOV M,D	9D	SBB L	C8	RZ	F3	DI
1D	DRC E	48	MOV C,B	73	MOV M,E	9E	SBB M	C9	RET Adr	F4	CP Adr
1E	MVI E,D8	49	MOV C,C	74	MOV M,H	9F	SBB A	CA	JZ	F5	PUSH PSW
1F	RAR	4A	MOV C,D	75	MOV M,L	A0	ANA B	CB	– –	F6	ORI D8
20	RIM	4B	MOV C,E	76	HLT	A1	ANA C	CC	CZ Adr	F7	RST 6
21	LXI H,D16	4C	MOV C,H	77	MOV M,A	A2	ANA D	CD	CALL Adr	F8	RM
22	SHLD Adr	4D	MOV C,L	78	MOV A,B	A3	ANA E	CE	ACI D8	F9	SPHL
23	INX H	4E	MOV C,M	79	MOV A,C	A4	ANA H	CF	RST 1	FA	JM Adr
24	INR H	4F	MOV C,A	7A	MOV A,D	A5	ANA L	D0	RNC	FB	EI
25	DCR H	50	MOV D,B	7B	MOV A,E	A6	ANA M	D1	POP D	FC	CM Adr
26	MVI H,D8	51	MOV D,C	7C	MOV A,H	A7	ANA A	D2	JNC Adr	FD	– –
27	DAA	52	MOV D,D	7D	MOV A,L	A8	XRA B	D3	OUT D8	FE	CPI D8
28	– –	53	MOV D,E	7E	MOV A,M	A9	XRA C	D4	CNC Adr	FF	RST 7
29	DAD H	54	MOV D,H	7F	MOV A,A	AA	XRA D	D5	PUSH D		
2A	LHLD Adr	55	MOV D,L	80	ADD B	AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity. D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. Adr = 16-bit address.

THIS IS THE LAST PRINTED PAGE.