2201/303
2203/303
2206/303
MICROPROCESSOR SYSTEMS
Oct./Nov. 2010
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN ELECTRONICS ENGINEERING
DIPLOMA IN TELECOMMUNICATIONS ENGINEERING
DIPLOMA IN INSTRUMENTATION AND CONTROL ENGINEERING

MICROPROCESSOR SYSTEMS

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:

Answer booklet;
8080/85 Microprocessor instruction set
Electronic calculator

Answer any **FIVE** *of the* **EIGHT** *questions in this paper.*
All questions carry equal marks.
Maximum marks of each part of a question are as shown.

This paper consists of 7 printed pages.

**Candidates should check the question paper to ascertain that all the
pages are printed as indicated and that no questions are missing.**

1. (a) Draw a labelled block diagram of a microcomputer and state the function (s) of each block. (10 marks)

(b) With the aid of a timing diagram, describe a memory read cycle. (7 marks)

(c) State the function of each of the following microprocessor registers;

(i) program counter;
(ii) instruction register;
(iii) stack pointer (3 marks)

2. (a) Table 1 shows a program listing in 8085 hexadecimal code.

(i) di-assemble the program into mnemonic form;

(ii) create the program execution trace table and determine the contents of HL at the end of program execution;

(iii) explain what the program accomplishes. (12 marks)

Table 1

Location (Hex)	Instruction (Hex)
1800	11
1801	0C
1802	00
1803	21
1804	00
1805	00
1806	06
1807	03
1808	19
1809	05
180A	C2
180B	08
180C	18
180D	76

(b) For each of the 8085 instructions in table 2.

(i) identify the addressing mode;
(ii) state the size, in bytes, of the instruction machine code. (8 marks)

Table 2

I.	LDA	1900H
II.	MOV	M,A
III	ADI	3EH
IV	CMA	

3. (a) Define the following as applied to memories:

(i) volatile;
(ii) random access.   (2 marks)

(b) A 4K x 8 memory is to be implemented using 1K x 4 memory chips.
Determine the number of:

(i) 1k x 4 memory chips required.
(ii) address lines required to address:

I   each chip;
II   the whole memory.

(iii) draw a schematic block diagram of the memory implementation.
                                                                                    (8 marks)

(c) (i) Define the following as applied to hard disk:

I   boot sector;
II   platter.

(ii) A hard-disk drive has 10 surfaces available for recording. Each surface consists
of 120 concentric tracks and the disk rotates at 1500 rpm. Each track is divided
into 16 blocks of 256 bytes. There is one read/write head per surface and it is
possible to read 10 tracks of a given cylinder. Determine the:

I   total capacity of the disk drive, in kilobytes;
II   maximum data transfer rate, in bits/sec.
                                                                                    (10 marks)

4. (a) (i) With the aid of a flowchart, write an assembly language sub-routine that does the division of two 8-bit numbers by successive subtraction.

   (ii) Write a main program that utilizes the subroutine in a (i) to divide the decimal number 99 by 7, then store the quotient in memory location 2000H and the remainder at memory location 2001H. (12 marks)

   (b) (i) State the **three** methods of parameter passing in sub-routine programming.

   (ii) Write a series of stack operations to exchange data between register pairs BC and HL.

   (iii) state any **one** disadvantage of programming using sub-routines. (8 marks)

5. (a) State any **two** internal conditions that may cause interrupts to a microprocessor. (2 marks)

   (b) (i) With the aid of a flowchart, enumerate the sequence of events that occur after a maskable interrupt.

   (ii) State **three** methods of implementing priority to an interrupt system. (9 marks)

   (c) With reference to Figure 1.

```
        PA3  ▭ 1              40 ▭ PA4
        PA2  ▭ 2              39 ▭ PA5
        PA1  ▭ 3              38 ▭ PA6
        PA0  ▭ 4              37 ▭ PA7
        RD   ▭ 5              36 ▭ WR
        CS   ▭ 6              35 ▭
        GND  ▭ 7              34 ▭ RESET
        A1   ▭ 8              33 ▭ D1
        A0   ▭ 9              32 ▭ D2
        PC7  ▭ 10             31 ▭ D3
        PC6  ▭ 11             30 ▭ D4
        PC5  ▭ 12             29 ▭ D5
        PC4  ▭ 13             28 ▭ D6
        PC0  ▭ 14             27 ▭ D7
        PC1  ▭ 15             26 ▭ Vcc
        PC2  ▭ 16             25 ▭ PB7
        PC3  ▭ 17             24 ▭ PB6
        PB0  ▭ 18             23 ▭ PB5
        PB1  ▭ 19             22 ▭ PB4
        PB2  ▭ 20             21 ▭ PB3
```
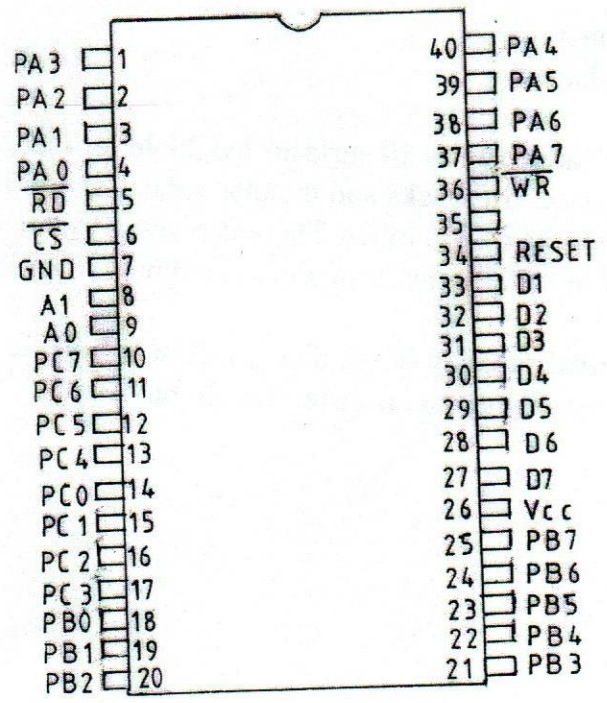
Fig. 1

(i)   identify the device;

(ii)   explain its function in a microcomputer.

(iii) For the signals $\overline{CS}$, RESET, PAO– PA7:

        I.   state the function of each;

        II.   list the device/signal EACH signal would typically be connected to in a system.

                              (9 marks)

6. (a) State any **three** concepts which define the sequential computer architecture.

                              (3 marks)

(b) Table 3 shows the listing of a delay program.

Determine:

(i)   program delay time, if the clock frequency is 5MHz;

(ii)   number of memory locations occupied by the program machine code.

                              (10 marks)

Table 3

Mnemonic	8088 T- states
LX1B, 1000H	10
LOOP: DCX B	6
XTHL	16
XTHL	16
NOP	4
NOP	4
MOV A, B	4
ORA C	4
JNZ LOOP	10/7

(c) (i)   State any **one** advantage of memory-mapped input/outputs.

(ii) Write an assembly language program that alternatively tests the status register of two devices as follows: when bit 0 of the status register is found to be 1, then a byte of data is brought in from the corresponding device. If bit 0 of either status register is zero, the inputting process ceases. The status registers have port addresses 24H and 36H and the corresponding buffer registers have addresses 26H and 38H respectively. The input data is to be stored into memory buffers beginning at BUFF1 and BUFF2 respectively.

                              (7 marks)

7. (a) (i) Develop a flowchart to outline the sequence of steps followed in developing a modern microprocessor based system.

(ii) Distinguish between a laptop computer and an embedded computer.

(10 marks)

(b) An 8-bit micro-processor-based system is used to measure system temperature changes. The temperature sensor has a sensitivity of 5mV/°C. The 8-bit analogue-to-digital converter (ADC) has two control lines labelled SC (start conversion) and EOC (end-of-conversion). The ADC has an input range of 0 - 5V.

(i) for the ADC, determine its maximum detectable input temperature;
(ii) draw a block schematic diagram to show how the temperature sensor, the ADC, and any extra hardware can be connected to provide the required data acquisition system.
(iii) develop a flowchart to control the data acquisition system in b(ii).

(10 marks)

8. (a) Develop a flowchart, to outline the logical method of tracing a fault in a microprocessor based system.

(8 marks)

(b) A RAM BOARD has address range:

4000 H – BFFFH.

(i) determine the amount of RAM on the board;

(ii) write an assembly language segment to test the RAM.

(9 marks)

(c) List any **three** equipment used to fault diagnose a modern microprocessor.

(3 marks)

8085 INSTRUCTION SET

Opcode	Instruction	Opcode	Instruction	Opcode	Instruction
00	NOP	2B	DCX H	56	MOV D,M
01	LXI B,d16	2C	INR L	57	MOV D,A
02	STAX B	2D	DCR L	58	MOV E,B
03	INX B	2E	MVI L,d8	59	MOV E,C
04	INR B	2F	CMA	5A	MOV E,D
05	DCR B	30	SIM	5B	MOV E,E
06	MVI B,d8	31	LXI SP,d16	5C	MOV E,H
07	RLC	32	STA adr16	5D	MOV E,L
08	DSUB	33	INX SP	5E	MOV E,M
09	DAD B	34	INR M	5F	MOV E,A
0A	LDAX B	35	DCR M	60	MOV H,B
0B	DCX B	36	MVI M,d8	61	MOV H,C
0C	INR C	37	STC	62	MOV H,D
0D	DCR C	38	LDSI index8	63	MOV H,E
0E	MVI C,d8	39	DAD SP	64	MOV H,H
0F	RRC	3A	LDA adr16	65	MOV H,L
10	ARHL	3B	DCX SP	66	MOV H,M
11	LXI D,d16	3C	INR A	67	MOV H,A
12	STAX D	3D	DCR A	68	MOV L,B
13	INX D	3E	MVI A,d8	69	MOV L,C
14	INR D	3F	CMC	6A	MOV L,D
15	DCR D	40	MOV B,B	6B	MOV L,E
16	MVI D,d8	41	MOV B,C	6C	MOV L,H
17	RAL	42	MOV B,D	6D	MOV L,L
18	RDEL	43	MOV B,E	6E	MOV L,M
19	DAD D	44	MOV B,H	6F	MOV L,A
1A	LDAX D	45	MOV B,L	70	MOV M,B
1B	DCX D	46	MOV B,M	71	MOV M,C
1C	INR E	47	MOV B,A	72	MOV M,D
1D	DCR E	48	MOV C,B	73	MOV M,E
1E	MVI E,d8	49	MOV C,C	74	MOV M,H
1F	RAR	4A	MOV C,D	75	MOV M,L
20	RIM	4B	MOV C,E	76	HLT
21	LXI H,d16	4C	MOV C,H	77	MOV M,A
22	SHLD adr16	4D	MOV C,L	78	MOV A,B
23	INX H	4E	MOV C,M	79	MOV A,C
24	INR H	4F	MOV C,A	7A	MOV A,D
25	DCR H	50	MOV D,B	7B	MOV A,E
26	MVI H,d8	51	MOV D,C	7C	MOV A,H
27	DAA	52	MOV D,D	7D	MOV A,L
28	LDHI index8	53	MOV D,E	7E	MOV A,M
29	DAD H	54	MOV D,H	7F	MOV A,A
2A	LHLD adr16	55	MOV D,L	80	ADD B

Opcode	Instruction	Opcode	Instruction	Opcode	Instruction
81	ADD C	AC	XRA H	D7	RST 2
82	ADD D	AD	XRA L	D8	RC
83	ADD E	AE	XRA M	D9	SHLX
84	ADD H	AF	XRA A	DA	JC adr16
85	ADD L	B0	ORA B	DB	IN adr8
86	ADD M	B1	ORA C	DC	CC adr16
87	ADD A	B2	ORA D	DD	JNX5 adr16
88	ADC B	B3	ORA E	DE	SBI d8
89	ADC C	B4	ORA H	DF	RST 3
8A	ADC D	B5	ORA L	E0	RPO
8B	ADC E	B6	ORA M	E1	POP H
8C	ADC H	B7	ORA A	E2	JPO adr16
8D	ADC L	B8	CMP B	E3	XTHL
8E	ADC M	B9	CMP C	E4	CPO adr16
8F	ADC A	BA	CMP D	E5	PUSH H
90	SUB B	BB	CMP E	E6	ANI d8
91	SUB C	BC	CMP H	E7	RST 4
92	SUB D	BD	CMP L	E8	RPE
93	SUB E	BE	CMP M	E9	PCHL
94	SUB H	BF	CMP A	EA	JPE adr16
95	SUB L	C0	RNZ	EB	XCHG
96	SUB M	C1	POP B	EC	CPE adr16
97	SUB A	C2	JNZ adr16	ED	LHLX
98	SBB B	C3	JMP adr16	EE	XRI d8
99	SBB C	C4	CNZ adr16	EF	RST 5
9A	SBB D	C5	PUSH B	F0	RP
9B	SBB E	C6	ADI d8	F1	POP PSW
9C	SBB H	C7	RST 0	F2	JP adr16
9D	SBB L	C8	RZ	F3	DI
9E	SBB M	C9	RET	F4	CP adr16
9F	SBB A	CA	JZ adr16	F5	PUSH PSW
A0	ANA B	CB	RSTV	F6	ORI d8
A1	ANA C	CC	CZ adr16	F7	RST 6
A2	ANA D	CD	CALL adr16	F8	RM
A3	ANA E	CE	ACI d8	F9	SPHL
A4	ANA H	CF	RST 1	FA	JM adr16
A5	ANA L	D0	RNC	FB	EI
A6	ANA M	D1	POP D	FC	CM adr16
A7	ANA A	D2	JNC adr16	FD	JX5 adr16
A8	XRA B	D3	OUT adr8	FE	CPI d8
A9	XRA C	D4	CNC adr16	FF	RST 7
AA	XRA D	D5	PUSH D		
AB	XRA E	D6	SUI d8		