2201/303
2203/303
2206/303
MICROPROCESSOR SYSTEMS
Oct./Nov. 2009
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN ELECTRONIC ENGINEERING
DIPLOMA IN TELECOMMUNICATION ENGINEERING
DIPLOMA IN INSTRUMENTATION AND CONTROL ENGINEERING

MICROPROCESSOR SYSTEMS

3 hours

INSTRUCTIONS TO CANDIDATES

Candidates should have the following for this examination:

Answer booklet;
8080/85 Microprocessor Instruction Set.
Electronic calculator.

*Answer any **FIVE** of the **EIGHT** questions in this paper.*
All questions carry equal marks.

This paper consists of 8 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

1. (a) Write assembly language program segments to perform each of the following:

(i) 2749H
+3A4BH

(ii) $24_{10} \times 8_{10}$

(iii) $108_{10} \div 4_{10}$ (12 marks)

(b) (i) Table 1 shows the ASCII code for the decimal numbers 0 - 9 in memory. Write an assembly language program segment that:

- reads a one digit decimal number from port 21H;
- uses the look-up **Table 1** to convert it into ASCII;
- displays the result on a display connected to port 22H.

(ii) State the **two** advantages of using look-up tables to convert data between codes. (8 marks)

Table 1

Memory location (Hex)	ASCII code (Hex)
2000	30
2001	31
2002	32
2003	33
2004	34
2005	35
2006	36
2007	37
2008	38
2009	39

2. (a) Tabulate the contrasts between the architectures of 8 - bit and 16 - bit microprocessors under the following:

(i) instruction set;
(ii) registers;
(iii) instruction fetching. (6 marks)

(b) Describe the following microprocessor signals:

(i) reset-out;
(ii) ready;
(iii) bus acknowledge.

(6 marks)

(c) A digital computer has a memory unit with 24 - bits per location. The instruction set consists of 190 different operations. Each instruction is stored in one location in memory and consists of an operation-code part and an address part. Determine the:

(i) number of bits needed for the operation code;
(ii) number of bits needed for address part of the operation;
(iii) the range of binary address that can be stored if it is:

I. unsigned;
II. signed, two's complement. (8 marks)

3. (a) A microprocessor system has 32-address lines and 16-data lines. Determine the:

(i) maximum number of addressable memory locations;
(ii) word size;
(iii) capacity of the microprocessor in bytes. (5 marks)

(b) **Figure 1** shows part of a microprocessor system containing a Random Access Memory (RAM), a Read Only Memory (ROM) and a serial input/output port.
Determine the simplified boolean expressions for the three chip enable signals (CEA, CEB, and CEC) to ensure that the devices respond only to the address ranges given in **table 2.** (9 marks)

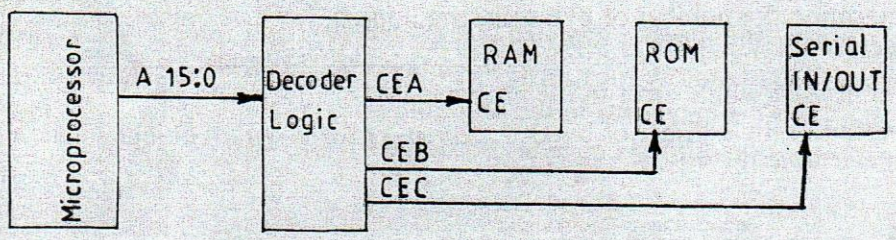

Figure 1

Table 2

Device	Address Range (Hexadecimal)
RAM	OOOO - BFFF
ROM	COOO - EFFF
Serial I/O port	FFOO - FFO7

(c) (i) Define the following as applied to hard-disks:

I. cylinder;
II. cluster.

(ii) A hard-disk drive has 8 sides, 614 tracks/side, 30 sectors/track and 512 bytes/sector.
Determine for the disk:

I. the total number of sectors;
II. the disk capacity, in Kilobytes.

(6 marks)

4. (a) Define the following microprocessor addressing modes, stating an example of instruction using the mode in each case:

(i) implied;
(ii) register indirect.

(4 marks)

(b) The program of **Table 3** adds bytes stored in memory then also saves the result in memory. For the program:

(i) determine the number of bytes that are added;
(ii) specify the memory locations where the result is stored;
(iii) identify the single error in the program;
(iv) determine the number of bytes occupied by the program object code.

(8 marks)

Table 3

LABEL	INSTRUCTION
	LXI H, 0000H LXI D, 0900H
NEXT:	ADD M JNC SKIP INR E

SKIP:	INX H
	DCR D
	JNZ NEXT
	LXI H, 009IH
	MOV M, A
	INX H
	MOV M, E
	HLT

(c) **Table 4** shows the contents of registers, at the start of program execution. Show the contents of the stack and SP after each instruction execution in **Table 5**.

(8 marks)

Table 4

Register	Contents(Hex)
BC	1234
DE	CDEF
HL	1100
SP	20C2

Table 5

PUSH D
PUSH H
PUSH B
POP D

5. (a) With the aid of a schematic block diagram, describe the operation of a 4-bit successive approximation analogue - to - digital converter. (8 marks)

(b) **Figure 2** shows a block diagram of an 8155 programmable input-output (PI0).

(i) If the PIO's base address is 40H, write and assembly language program segment that will:

- read port A(41H) and port C(43H) of the PI0 to form a 14-bit number (port A is the LSB source);
- load this number into the PI0's timer;
- place the timer into continuous operation.

(ii) If the timer clock is 100KHZ, determine the number to be loaded into the timer register to achieve a single square wave pulses every 500μS.

(iii) With the aid of a labelled diagram, show how you would interface two(2) seven-segment LED digits to the PIO's ports A and B.

(12 marks)

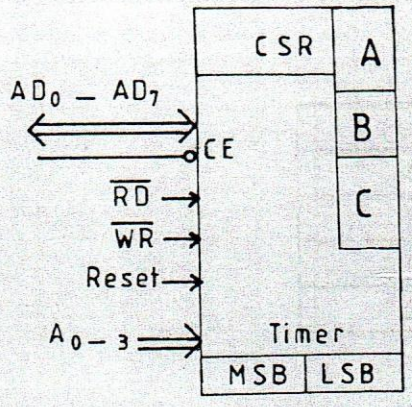

Figure 2

6. (a) In place of an operating system, 8-bit development systems have a monitor program. State any **four** monitor program facilities and explain the function(s) of each. (8 marks)

(b) Explain any **three** benefits of using a development system when implementing a microprocessor based system. (6 marks)

(c) With the aid of flowchart segments, illustrate the following programming structures:

(i) while.....loop;

(ii) sequence. (6 marks)

7. (a) (i) Describe the hardware interrupts of the 8085 microprocessor.

(ii) List the interrupts in a(i) in descending order of priority. (8 marks)

(b) **Table 6** lists five statements describing the methods in which a microprocessor handles interrupt requests when interfaced with a Programmable Interrupt Controller (PIC). Rearrange the list according to the order in which the statements should occur. (5 marks)

Table 6

1. The PIC signals the microprocessor that an interrupt has occurred.
2. The microprocessor communicates with the interrupting device, then executes the interrupt service routine.
3. A device generates an interrupt and sends the request to the PIC.
4. The PIC reports the priority level of the interrupt to the microprocessor.
5. The microprocessor requests the priority level of the interrupt from the PIC.

(c) Write a subroutine program to perform the following threshold detection:

- If register A > NUM1, return +1 in register A.
- If register A = NUM1, return 0 in register A.
- If register A < NUM1, return -1 in register A.

Assume the data, NUM1 is an 8-bit signed number and it will be initialised at run time in register B. (7 marks)

8. (a) Describe the procedure of testing each of the following, in a microcomputer, using a multimeter:

(i) open-circuit in a resistor;
(ii) d.c voltage level. (8 marks)

(b) **Figure 3** shows the input/output hardware needed to test a AND gate. With the aid of a flowchart, write an assembly language program segment to generate the input conditions to the AND gate and activate LED1 if the test fails, else activate LED2 if the gate is good. (12 marks)

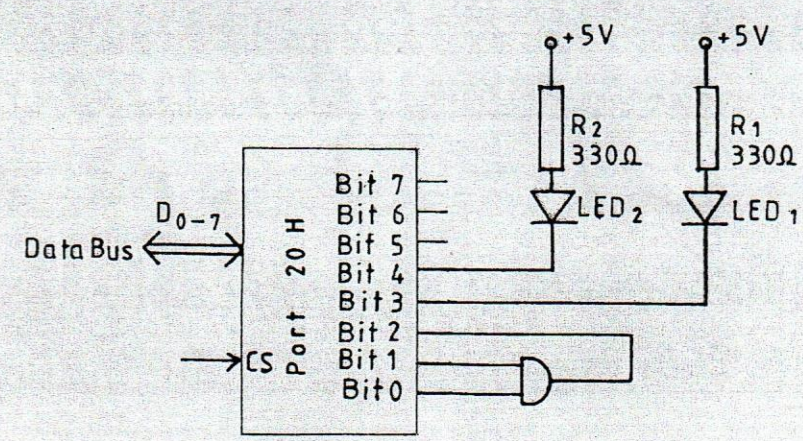

Figure 3

TABLE: 8085 INSTRUCTION SET

00	NOP	2B	DCX	H	56	MOV	D,M	81	ADD	C	AC	XRA	H	D7	RST	2
01	LXI	2C	INR	L	57	MOV	D,A	82	ADD	D	AD	XRA	L	D8	RC	
02	STAX	2D	DCR	L	58	MOV	E,B	83	ADD	E	AE	XRA	M	D9	SHLX	
03	INX	2E	MVI	L,d8	59	MOV	E,C	84	ADD	H	AF	XRA	A	DA	JC	adr16
04	INR	2F	CMA		5A	MOV	E,D	85	ADD	L	B0	ORA	B	DB	IN	adr8
05	DCR	30	SIM		5B	MOV	E,E	86	ADD	M	B1	ORA	C	DC	CC	adr16
06	MVI	31	LXI	SP,d16	5C	MOV	E,H	87	ADD	A	B2	ORA	D	DD	JNX5	adr16
07	RLC	32	STA	adr16	5D	MOV	E,L	88	ADC	B	B3	ORA	E	DE	SBI	d8
08	DSUB	33	INX	SP	5E	MOV	E,M	89	ADC	C	B4	ORA	H	DF	RST	3
09	DAD	34	INR	M	5F	MOV	E,A	8A	ADC	D	B5	ORA	L	E0	RPO	
0A	LDAX	35	DCR	M	60	MOV	H,B	8B	ADC	E	B6	ORA	M	E1	POP	H
0B	DCX	36	MVI	M,d8	61	MOV	H,C	8C	ADC	H	B7	ORA	A	E2	JPO	adr16
0C	INR	37	STC		62	MOV	H,D	8D	ADC	L	B8	CMP	B	E3	XTHL	
0D	DCR	38	LDSI	index8	63	MOV	H,E	8E	ADC	M	B9	CMP	C	E4	CPO	adr16
0E	MVI	39	DAD	SP	64	MOV	H,H	8F	ADC	A	BA	CMP	D	E5	PUSH	H
0F	RRC	3A	LDA	adr16	65	MOV	H,L	90	SUB	B	BB	CMP	E	E6	ANI	d8
10	ARHL	3B	DCX	SP	66	MOV	H,M	91	SUB	C	BC	CMP	H	E7	RST	4
11	LXI	3C	INR	A	67	MOV	H,A	92	SUB	D	BD	CMP	L	E8	RPE	
02	STAX	3D	DCR	A	68	MOV	L,B	93	SUB	E	BE	CMP	M	E9	PCHL	
13	INX	3E	MVI	A,d8	69	MOV	L,C	94	SUB	H	BF	CMP	A	EA	JPE	adr16
14	INR	3F	CMC		6A	MOV	L,D	95	SUB	L	C0	RNZ		EB	XCHG	
15	DCR	40	MOV	B,B	6B	MOV	L,E	96	SUB	M	C1	POP	B	EC	CPE	adr16
16	MVI	41	MOV	B,C	6C	MOV	L,H	97	SUB	A	C2	JNZ	adr16	ED	LHLX	
17	RAL	42	MOV	B,D	6D	MOV	L,L	98	SBB	B	C3	JMP	adr16	EE	XRI	d8
18	RDEL	43	MOV	B,E	6E	MOV	L,M	99	SBB	C	C4	CNZ	adr16	EF	RST	5
19	DAD	44	MOV	B,H	6F	MOV	L,A	9A	SBB	D	C5	PUSH	B	F0	RP	
1A	LDAX	45	MOV	B,L	70	MOV	M,B	9B	SBB	E	C6	ADI	d8	F1	POP	PSW
1B	**DCX**	**46**	**MOV**	**B,M**	**71**	**MOV**	**M,C**	**9C**	**SBB**	**H**	**C7**	**RST**	**0**	**F2**	**JP**	**adr16**
1C	**INR**	47	MOV	B,A	72	MOV	M,D	9D	SBB	L	C8	RZ		F3	DI	
1D	DCR	48	MOV	C,B	73	MOV	M,E	9E	SBB	M	C9	RET		F4	CP	adr16
1E	MVI	49	MOV	C,C	74	MOV	M,H	9F	SBB	A	CA	JZ	adr16	F5	PUSH	PSW
1F	RAR	4A	MOV	C,D	75	MOV	M,L	A0	ANA	B	CB	RSTV		F6	ORI	d8
20	RIM	4B	MOV	C,E	76	HLT		A1	ANA	C	CC	CZ	adr16	F7	RST	6
21	LXI	4C	MOV	C,H	77	MOV	M,A	A2	ANA	D	CD	CALL	adr16	F8	RM	
22	SHLD	4D	MOV	C,L	78	MOV	A,B	A3	ANA	E	CE	ACI	d8	F9	SPHL	
23	INX	4E	MOV	C,M	79	MOV	A,C	A4	ANA	H	CF	RST	1	FA	JM	adr16
24	INR	4F	MOV	C,A	7A	MOV	A,D	A5	ANA	L	D0	RNC		FB	EI	
25	DCR	50	MOV	D,B	7B	MOV	A,E	A6	ANA	M	D1	POP	D	FC	CM	adr16
26	MVI	51	MOV	D,C	7C	MOV	A,H	A7	ANA	A	D2	JNC	adr16	FD	JX5	adr16
27	DAA	52	MOV	D,D	7D	MOV	A,L	A8	XRA	B	D3	OUT	adr8	FE	CPI	d8
28	LDHI	index8	53	MOV	D,E	7E	MOV	A,M	A9	XRA	C	D4	CNC	adr16	FF	RST	7
29	DAD	H	54	MOV	D,H	7F	MOV	A,A	AA	XRA	D	D5	PUSH	D		
2A	LHLD	adr16	55	MOV	D,L	80	ADD	B	AB	XRA	E	D6	SUI	d8		