2201/303
2203/303
2206/303
MICROPROCESSOR SYSTEMS
Oct./Nov. 2008
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN ELECTRONIC ENGINEERING
DIPLOMA IN TELECOMMUNICATION ENGINEERING
DIPLOMA IN INSTRUMENTATION AND CONTROL ENGINEER

MICROPROCESSOR SYSTEMS

3 hours

INSTRUCTIONS TO CANDIDATES

Candidates should have the following for this examination:

Answer booklet.
8080/85 Microprocessor Instruction Set.
Mathematical tables/calculator.

*Answer any **FIVE** of the following **EIGHT** questions.*
All questions carry equal marks.

This paper consists of 9 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and no questions are missing.

Turn over

1. (a) With the aid of one line instructions, define the following microprocessor addressing modes:

(i) direct;
(ii) register;
(iii) immediate. (6 marks)

(b) For the program in Table 1:

(i) generate the Hexadecimal machine code;
(ii) determine the execution time in T-states;
(iii) specify the values of the following registers after the execution of the STA instruction.

I. A
II. PC
III. HL (14 marks)

Table 1

		T-States
	ORG COOOH	
	XRA A	4
	LHLD LIST	16
LOOP:	MVI B, COUNT	7
	NOP	4
	NOP	4
	DCR B	4
	JNZ LOOP	7/10
	STA MEM	13
	HLT	5
	ORG DOOOH	
LIST	DB 2, 4, 6, 8, 10	
COUNT	DB 7	
MEM:	DS 2	
	END	

2. (a) Differentiate between isolated and memory-mapped input-output ports. (4 marks)

(b) (i) Figure 1 shows parts of a microprocessor based system. Use the parts to draw a complete system showing all interconnections.

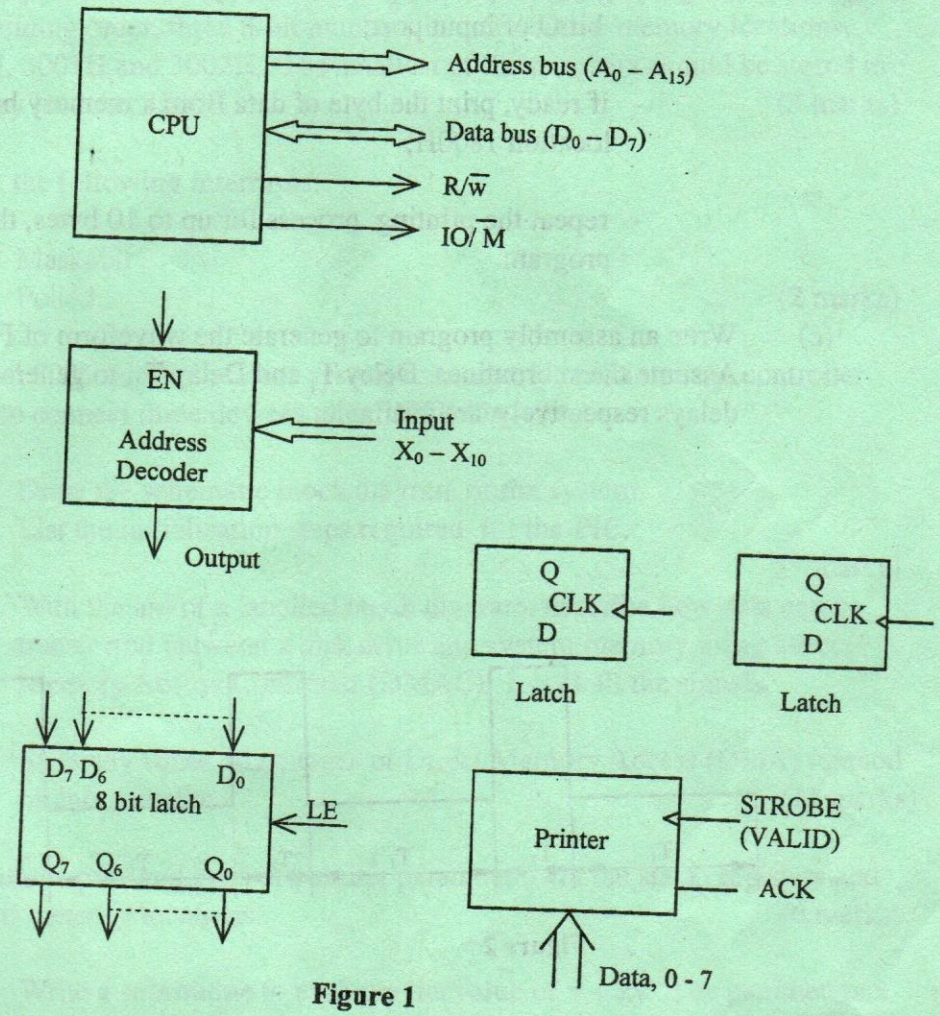

Figure 1

(b) (ii) If for figure 1, the printer port addresses are

input = 21H
output = 22H

Write a subroutine program to perform the following:

- test whether the printer is ready to receive a byte of data, by testing bit O of input port;
- if ready, print the byte of data from a memory buffer starting from location 1800H;
- repeat the printing process for up to 10 bytes, then return to main program. (12 marks)

(c) Write an assembly program to generate the waveform of Figure 2 at port 24H. Assume the subroutines, Delay T_1 and Delay T_2, to generate the T_1 and T_2 delays respectively, are available. (4 marks)

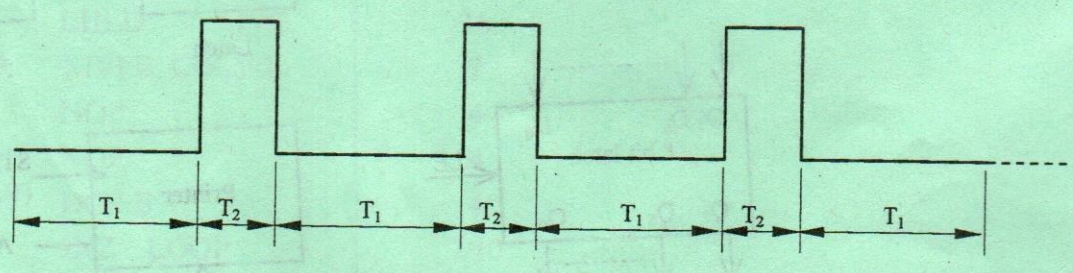

Figure 2

3. (a) With the aid of flowchart segments, describe the following programming structures:

(i) Decision;
(ii) Repetition/iteration.

(6 marks)

(b) Write an assembly language program to perform the following:

- add two BCD numbers 98 and 67;
- subtract the BCD number 56 from the corrected result;
- store the BCD result in memory location 200C H.

(6 marks)

(c) With the aid of a flowchart, write an assembly language program to arrange in ascending order, three 8-bit numbers in consecutive memory locations 3000H, 3001H and 3002H. The smallest of the numbers should be stored in memory location 3000H.

(8 marks)

4. (a) Define the following interrupts:

(i) Maskable;
(ii) Polled.

(2 marks)

(b) An intel 8085 microprocessor system uses a peripheral interrupt controller (PIC) to connect three devices to its INTR Pin.

(i) Draw the schematic block diagram of the system.
(ii) List the initialisation steps required for the PIC.

(7 marks)

(c) (i) With the aid of a labelled block diagram, describe how data can be transferred between a disk drive and system memory using Direct Memory Access Controller (DMAC). Label all the signals.

(ii) State any **three** advantages of Direct Memory Access (DMA) method of data transfer.

(11 marks)

5. (a) Explain the pros and cons of passing parameters via the stack, registers and explicit memory locations.

(6 marks)

(b) (i) Write a subroutine to evaluate the value of $x + 2y$. The parameters x and y are each 8-bit and both are passed to the subroutine by registers. The result is an 8-bit number that is passed by memory reference. Save any working registers onto the stack during subroutine processing.

(ii) Draw a memory map of the stack during subroutine execution in b(i). Assume the stack pointer (SP) has the data 3000H after subroutine call.

(10 marks)

(c) For each item in column 'A' of Table 2, select the matching entry in column 'B'. (4 marks)

Table 2

A	B
TRI-STATE	Ignores CPU interrupt enable bit
NMI	Bus Request/Grant
PIC	Data Bus
DMA	Controls IRQ priority

6. (a) (i) Draw a labelled block diagram of a basic Microprocessor Development System(MDS).

(ii) Describe the functions of the following facilities in an MDS:

I. Single-stepping
II. Break-point
III. Manual-mode (11 marks)

(b) (i) State any **three** advantages of using an In-Circuit-Emulator (ICE) in microprocessor development.

(ii) Describe any **three** RS-232 interface signals. (9 marks)

7. (a) (i) For a 128K x 16 memory device, determine the following:

I. word size
II. number of address lines

(ii) Determine the address range mapped by the following expression:

$$CE = \overline{A}_{15} \times A_{14} \times A_{13} \times \overline{A}_{12} \times A_{11} \times A_{10}$$ (6 marks)

(b) The diagram of Figure 3 shows a microcomputer memory map.

(i) Determine the amount of memory dedicated to:

I. RAM
II. EPROM

(ii) Design a decoder scheme and implement the system memory using 4K x 8 EPROM and 4K x 4 RAM devices. (12 marks)

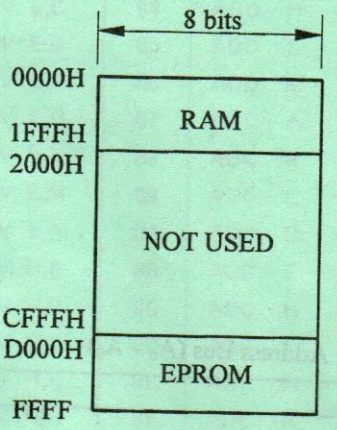

Figure 3

(c) State any **two** advantages of Dynamic RAM over static RAM memories. (2 marks)

8. (a) (i) Describe the checksum method of testing microcomputer ROM memories.

(ii) Explain the drawback of the method in a(i). (6 marks)

(b) Figure 4 shows the memory address decoding circuit for a microcomputer system.

(i) Determine the address range for each RAM device.

(ii) Explain the effect of each of the following on the circuit:

I. Line A_{11} becomes open circuit
II. Line A_{14} gets shorted to earth
III. Lines A_{14} and A_{15} are interchanged. (14 marks)

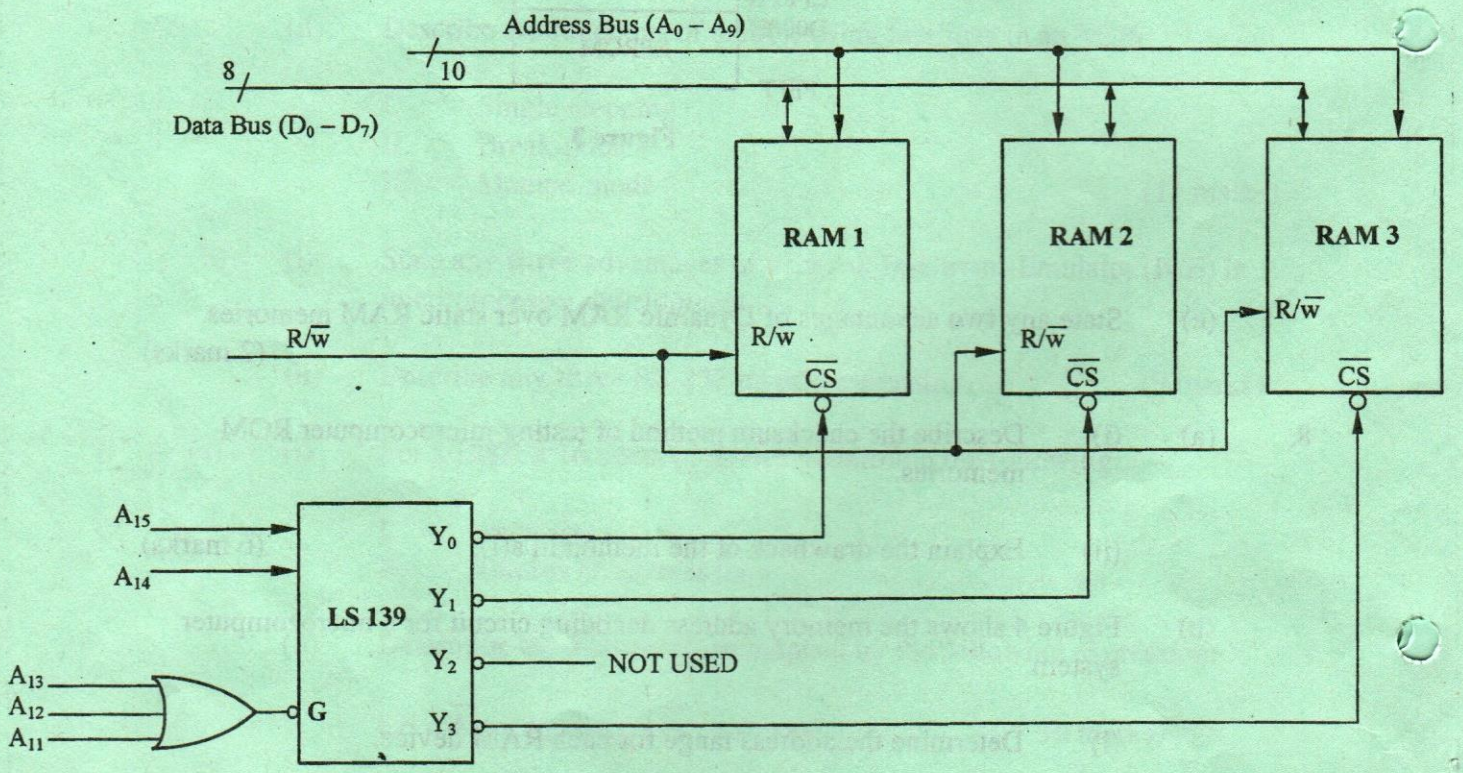
Address Bus ($A_0 - A_9$)
10
8
Data Bus ($D_0 - D_7$)
RAM 1
RAM 2
RAM 3
R/$\overline{w}$
$\overline{CS}$
A_{15}
A_{14}
A_{13}
A_{12}
A_{11}
LS 139
G
Y_0
Y_1
Y_2
Y_3
NOT USED

Figure 4

Instruction set of

8080/8085

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	2B	DCX H	56	MOV D,M	81	ADD C	AC	XRA H	D7	RST 2
01	LX1 B,D16	2C	INR L	57	MOV D,A	82	ADD D	AD	XRA L	D8	RC
02	STAX B	2D	DCR L	58	MOV E,B	83	ADD E	AE	XRA M	D9	–
03	INX B	2E	MVI L,D8	59	MOV E,C	84	ADD H	AF	XRA A	DA	JC Adr
04	INR B	2F	CMA	5A	MOV E,D	85	ADD L	B0	ORA B	DB	IN D8
05	DCR B	30	SIM	5B	MOV E,E	86	ADD M	B1	ORA C	DC	CC Adr
06	MVI B,D8	31	LXI SPD16	5C	MOV E,H	87	ADD A	B2	ORA D	DD	–
07	RLC	32	STA Adr	5D	MOV E,L	88	ADC B	B3	ORA E	DE	SBI D8
08	–	33	INX SP	5E	MOV E,M	89	ADC C	B4	ORA H	DF	RST 3
09	DAD B	34	INR M	5F	MOV E,A	8A	ADC D	B5	ORA L	E0	RPO
0A	LDAX B	35	DCR M	60	MOV H,B	8B	ADC E	B6	ORA M	E1	POP H
0B	DCX B	36	MVI M,D8	61	MOV H,C	8C	ADC H	B7	ORA A	E2	JPO Adr
0C	INR C	37	STC	62	MOV H,D	8D	ADC L	B8	CMP B	E3	XTHL
0D	DCR C	38	–	63	MOV H,E	8E	ADC M	B9	CMP C	E4	CPO Adr
0E	MVI C,D8	39	DAD SP	64	MOV H,H	8F	ADC A	BA	CMP D	E5	PUSH H
0F	RRC	3A	LDA Adr	65	MOV H,L	8G	SUB B	BB	CMP E	E6	ANI D8
10	–	3B	DCX SP	66	MOV H,M	91	SUB C	BC	CMP H	E7	RST 4
11	LXI D,D16	3C	INR A	67	MOV H,A	92	SUB D	BD	CMP L	E8	RPE
12	STAX D	3D	DCR A	68	MOV L,B	93	SUB E	BE	CMP M	E9	PCHL
13	INX D	3E	MVI A,D8	69	MOV L,C	94	SUB H	BF	CMP A	EA	JPE Adr
14	INR D	3F	CMC	6A	MOV L,D	95	SUB L	C0	RNZ	EB	XCHG
15	DCR D	40	MOV B,B	6B	MOV L,E	96	SUB M	C1	POP B	EC	CPE Adr
16	MVI D,D8	41	MOV B,C	6C	MOV L,H	97	SUB A	C2	JNZ Adr	ED	–
17	RAL	42	MOV B,D	6D	MOV L,L	98	SBB B	C3	JMP Adr	EE	ERI D8
18	–	43	MOV B,E	6E	MOV L,M	99	SBB C	C4	CNZ Adr	EF	RST 5
19	DAD D	44	MOV B,H	6F	MOV L,A	9A	SBB D	C5	PUSH B	F0	RP
1A	LDAX D	45	MOV B,L	70	MOV M,B	9B	SBB E	C6	ADI D8	F1	POP PSW
1B	DCX D	46	MOV B,M	71	MOV M,C	9C	SBB H	C7	RST 0	F2	JP Adr
1C	INR E	47	MOV B,A	72	MOV M,D	9D	SBB L	C8	RZ	F3	DI
1D	DRC E	48	MOV C,B	73	MOV M,E	9E	SBB M	C9	RET Adr	F4	CP Adr
1E	MVI E,D8	49	MOV C,C	74	MOV M,H	9F	SBB A	CA	JZ	F5	PUSH PSW
1F	RAR	4A	MOV C,D	75	MOV M,L	A0	ANA B	CB	–	F6	ORI D8
20	RIM	4B	MOV C,E	76	HLT	A1	ANA C	CC	CZ Adr	F7	RST 6
21	LXI H,D16	4C	MOV C,H	77	MOV M,A	A2	ANA D	CD	CALL Adr	F8	RM
22	SHLD Adr	4D	MOV C,L	78	MOV A,B	A3	ANA E	CE	ACI D8	F9	SPHL
23	INX H	4E	MOV C,M	79	MOV A,C	A4	ANA H	CF	RST 1	FA	JM Adr
24	INR H	4F	MOV C,A	7A	MOV A,D	A5	ANA L	D0	RNC	FB	E1
25	DCR H	50	MOV D,B	7B	MOV A,E	A6	ANA M	D1	POP D	FC	CM Adr
26	MVI H,D8	51	MOV D,C	7C	MOV A,H	A7	ANA A	D2	JNC Adr	FD	–
27	DAA	52	MOV D,D	7D	MOV A,L	A8	XRA B	D3	OUT D8	FE	CPI D8
28	–	53	MOV D,E	7E	MOV A,M	A9	XRA C	D4	CNC Adr	FF	RST 7
29	DAD H	54	MOV D,H	7F	MOV A,A	AA	XRA D	D5	PUSH D		
2A	LHLD Adr	55	MOV D,L	80	ADD B	AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity. D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. Adr = 16-bit address.