2201/303
2203/303
2206/303
MICROPROCESSOR SYSTEMS
Oct./ Nov. 2011
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN ELECTRONICS ENGINEERING
DIPLOMA IN TELECOMMUNICATIONS ENGINEERING
DIPLOMA IN INSTRUMENTATION AND CONTROL ENGINEERING

MICROPROCESSOR SYSTEMS

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:

Answer booklet;
8080/85 microprocessor instruction set;
Electronic calculator.

*Answer any **FIVE** of the **EIGHT** questions in this paper.*
***ALL** questions carry equal marks.*
Maximum marks for each part of a question are shown.

This paper consists of 8 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

1. (a) Draw a block diagram of an 8-bit microprocessor and state the function of each part. (7 marks)

(b) A hypothetical microprocessor has an instruction set as shown in Table 1.

(i) Using the microprocessor instruction set, write an assembly language program to perform the following:

6 + 9 - 4

(ii) With the aid of a trace table, determine the contents of the accumulator after the execution of the program in table 2. (9 marks)

Table 1.

OPcode (Hex)	Mnemonic	Explanation
BB	ADD L8	Add byte to Accumulator
FO	SUB L8	Subtract byte from Accumulator
4C	INC A	Increment the Accumulator
4A	DEC A	Decrement the Accumulator
F6	LD A, L8	Move byte into the Accumulator
96	STOP	Halt the microprocessor

Table 2.

Address (Hex)	OPcode (Hex)
8001	F6
8002	07
8003	FO
8004	03
8005	4C
8006	4C
8007	96

(c) Differentiate between:

(i) a mainframe computer and a microcomputer;

(ii) analogue and digital computer. (4 marks)

2. (a) Define the following as applied to memories:

(i) access time;

(ii) dynamic. (2 marks)

(b) An 8-bit microprocessor has a total addressable memory space of 64 Kbytes. The memory is organised such that the first 16 Kbytes is ROM, the next 8 Kbytes is reserved for future expansion, then followed by 32 Kbytes of RAM. The remaining space is also reserved for future expansion.

(i) Determine the:

I. number of address lines for the microprocessor;

II. total amount of memory reserved for future expansion.

(ii) Draw the microcomputer memory map, labelling the start and end addresses of each region, in hexadecimal.

(iii) If the available ROM chips are 8K x 8 and RAM chips are 8K x 8:

I. determine the number of chips required to implement each memory type;

II. draw a labelled schematic block diagram to illustrate the implementation of the memory map for the RAM only. (18 marks)

3 Table 3 shows an 8085 assembly language program.

Table 3

Line	Label	Instruction
1		ORG 11OOH
2		COUNT EQU 04 H
3		LX1 H, 115OH
4		MVI C, COUNT
5		XRA A
6	AGAIN:	ADD M
7		INX H
8		DCR C
9		JNZ AGAIN
10		STA MEM
11		HLT ORG 1150 H
12		DB 45H, 41H, 43H, 47H
13		ORG 1170 H
14	MEM:	DS 1
15		END

(a) List any **four** directives used in the program. (2 marks)

(b) Draw a flowchart for the program and explain the program's purpose. (8 marks)

(c) Determine the contents of registers A, H and L at the **end** of program execution. (6 marks)

(d) State how to modify the program to keep the purpose of the program if the instructions at line 11 and 12 are changed as shown in Table 4. (2 marks)

Table 4

13: ORG 2500H
16: DB 45H, 41H, 43H, 47H, 49H.

(e) State **two** advantages of low level language programs. (2 marks)

4. (a) With reference to instruction execution, define the following:

(i) instruction cycle;

(ii) machine cycle;

(iii) T-state. (3 marks)

(b) Table 5 shows a DELAY subroutine.

Table 5

Line	Label	Instruction	No. of T-states
1		LX1 H, 2000H	10
2	LOOP:	DCX H	6
3		NOP	4
4		NOP	4
5		MOV A, H	4
6		ORA L	4
7		JNZ LOOP	10/7
8		RET	10

(i) Assuming a clock frequency of 10 MHz, determine:

I. time of one T-state;

II. total time delay in executing the subroutine.

(ii) State the addressing modes for each of the instruction at lines 1, 2 and 7. (10 marks)

(c) With the aid of a flowchart, write an assembly language program which will copy a block of 10 bytes of data from RAM memory locations, starting at location 2000H to RAM locations starting at 3000H. (7 marks)

5. Figure 1 shows a water level measuring system. A 8085 microcomputer is connected to a level sensor, through an 8-bit analogue-to-digital converter, which gives 5V when the water tank is 100% full.

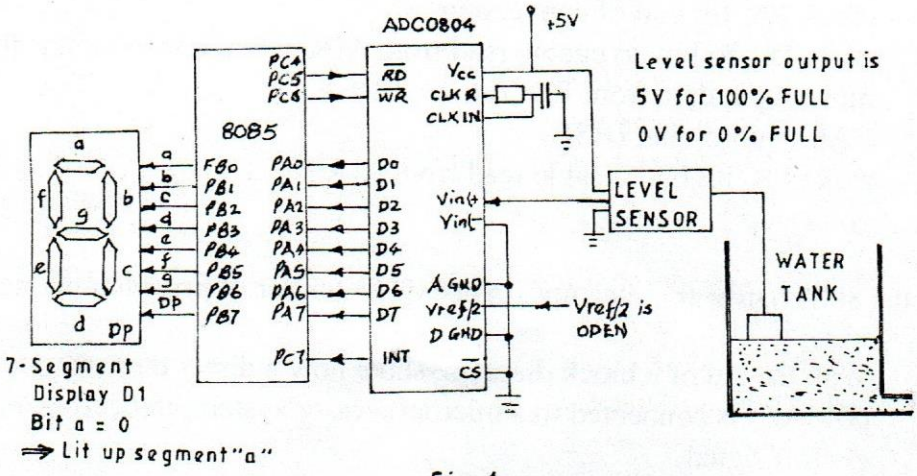

Fig. 1

(a) If the digital output (D_0 - D_7) of the ADC 0804 is E6H, determine the value of the sensor output voltage, Vin. (5 marks)

(b) Table 6 shows the system port configuration.

Table 6

Port Name	Address
Control (CSR)	40
Port A	41
Port B	42
Port C	43
Control byte (Port A = Input, Port B = Output, Port C = handshake) = 8AH	

(i) Write an 8085 assembly subroutine 'DISP' according to the following algorithm.

DISPLAY ROUTINE

1. compare the input tank level accumulator A with E6H
2. if A > E6H, display letter 'H' in the seven segment display D1, else display letter 'C'
3. call the subroutine 'DELAY'
4. return to main program.

NB: Assume the subroutine 'DELAY' is available.

(ii) Write the 8085 main program according to the following algorithm.

1. set port A as input, Port B as output and Port C as handshake
2. make PC_6 from low-to-high to start ADC conversion
3. check PA_7 for end of conversion
4. make PC_5 to low to enable read from ADC when conversion is finished
5. move input data from Port A to register A
6. CALL subroutine DISP
7. make PB_5 high to disable read from ADC
8. go to step 1. (15 marks)

6. (a) List the 8085 hardware interrupts in decreasing order of priority ranking. (5 marks)

(b) (i) With the aid of a block diagram, show how a direct memory Access controller (DMAC) is connected to a microprocessor system, indicating all the main control signal.

(ii) Outline the operation of the system in b(i). (8 marks)

(c) (i) Write an assembly language subroutine to generate the waveform of figure 2 (a). Assume that a delay subroutine is available.

(ii) Modify the program in c(i) to generate the waveform of fig 2 (b). (7 marks)

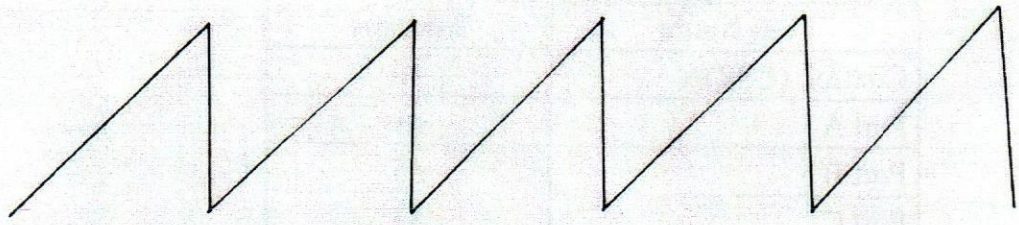

Fig. 2 (a)

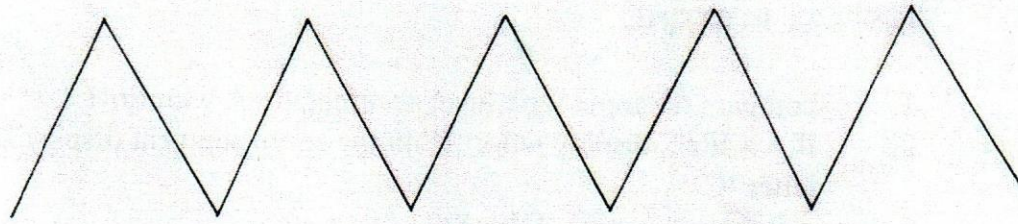

Fig 2 (b)

7. (a) (i) State the function of each of the following software development aid:

I. text editor;

II. debugger;

III. loader;

IV. macro instruction.

(ii) With the aid of a block diagram, describe how an in-circuit emulator (ICE) is used in the development of a microprocessor-based system. (12 marks)

(b) Describe any **four** functions of an operating system. (8 marks)

8. (a) Describe each of the following microcomputer troubleshooting aids:

(i) single-stepping;

(ii) break-point. (4 marks)

(b) State the function of each of the following 8085 microprocessor signals:

(i) IO/$\overline{M}$;

(ii) HOLD;

(iii) $\overline{INTA}$;

(iv) ALE. (5 marks)

(c) (i) With the aid of a diagram, describe how to test the correct operation of a TTL NOT gate.

(ii) Draw a block diagram of a logic analyser and state the function of each block. (11 marks)

Instruction set of

8080/8085

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	28	DCX H	56	MOV D,M	81	ADD C	AC	XRA H	D7	RST 2
01	LXI B,D16	2C	INR L	57	MOV D,A	82	ADD D	AD	XRA L	D8	RC
02	STAX B	2D	DCR L	58	MOV E,B	83	ADD E	AE	XRA M	D9	–
03	INX B	2E	MVI L,D8	59	MOV E,C	84	ADD H	AF	XRA A	DA	JC Adr
04	INR B	2F	CMA	5A	MOV E,D	85	ADD L	B0	ORA B	DB	IN D8
05	DCR B	30	SIM	5B	MOV E,E	86	ADD M	B1	ORA C	DC	CC Adr
06	MVI B,D8	31	LXI SPD16	5C	MOV E,H	87	ADD A	B2	ORA D	DD	–
07	RLC	32	STA Adr	5D	MOV E,L	88	ADC B	B3	ORA E	DE	SBI D8
08	–	33	INX SP	5E	MOV E,M	89	ADC C	B4	ORA H	DF	RST 3
09	DAD B	34	INR M	5F	MOV E,A	8A	ADC D	B5	ORA L	E0	RPO
0A	LDAX B	35	DCR M	60	MOV H,B	8B	ADC E	B6	ORA M	E1	POP H
0B	DCX B	36	MVI M,D8	61	MOV H,C	8C	ADC H	B7	ORA A	E2	JPO Adr
0C	INR C	37	STC	62	MOV H,D	8D	ADC L	B8	CMP B	E3	XTHL
0D	DCR C	38	– –	63	MOV H,E	8E	ADC M	B9	CMP C	E4	CPO Adr
0E	MVI C,D8	39	DAD SP	64	MOV H,H	8F	ADC A	BA	CMP D	E5	PUSH H
0F	RRC	3A	LDA Adr	65	MOV H,L	8G	SUB B	BB	CMP E	E6	ANI D8
10	– –	3B	DCX SP	66	MOV H,M	91	SUB C	BC	CMP H	E7	RST 4
11	LXI D,D16	3C	INR A	67	MOV H,A	92	SUB D	BD	CMP L	E8	RPE
12	STAX D	3D	DCR A	68	MOV L,B	93	SUB E	BE	CMP M	E9	PCHL
13	INX D	3E	MVI A,D8	69	MOV L,C	94	SUB H	BF	CMP A	EA	JPE Adr
14	INR D	3F	CMC	6A	MOV L,D	95	SUB L	C0	RNZ	EB	XCHG
15	DCR D	40	MOV B,B	6B	MOV L,E	96	SUB M	C1	POP B	EC	CPE Adr
16	MVI D,D8	41	MOV B,C	6C	MOV L,H	97	SUB A	C2	JNZ Adr	ED	– –
17	RAL	42	MOV B,D	6D	MOV L,L	98	SBB B	C3	JMP Adr	EE	ERI D8
18	– –	43	MOV B,E	6E	MOV L,M	99	SBB C	C4	CNZ Adr	EF	RST 5
19	DAD D	44	MOV B,H	6F	MOV L,A	9A	SBB D	C5	PUSH B	F0	RP
1A	LDAX D	45	MOV B,L	70	MOV M,B	9B	SBB E	C6	ADI D8	F1	POP PSW
1B	DCX D	46	MOV B,M	71	MOV M,C	9C	SBB H	C7	RST 0	F2	JP Adr
1C	INR E	47	MOV B,A	72	MOV M,D	9D	SBB L	C8	RZ	F3	DI
1D	DRC E	48	MOV C,B	73	MOV M,E	9E	SBB M	C9	RET Adr	F4	CP Adr
1E	MVI E,D8	49	MOV C,C	74	MOV M,H	9F	SBB A	CA	JZ	F5	PUSH PSW
1F	RAR	4A	MOV C,D	75	MOV M,L	A0	ANA B	CB	– –	F6	ORI D8
20	RIM	4B	MOV C,E	76	HLT	A1	ANA C	CC	CZ Adr	F7	RST 6
21	LXI H,D16	4C	MOV C,H	77	MOV M,A	A2	ANA D	CD	CALL Adr	F8	RM
22	SHLD Adr	4D	MOV C,L	78	MOV A,B	A3	ANA E	CE	ACI D8	F9	SPHL
23	INX H	4E	MOV C,M	79	MOV A,C	A4	ANA H	CF	RST 1	FA	JM Adr
24	INR H	4F	MOV C,A	7A	MOV A,D	A5	ANA L	D0	RNC	FB	EI
25	DCR H	50	MOV D,B	7B	MOV A,E	A6	ANA M	D1	POP D	FC	CM Adr
26	MVI H,D8	51	MOV D,C	7C	MOV A,H	A7	ANA A	D2	JNC Adr	FD	– –
27	DAA	52	MOV D,D	7D	MOV A,L	A8	XRA B	D3	OUT D8	FE	CPI D8
28	– –	53	MOV D,E	7E	MOV A,M	A9	XRA C	D4	CNC Adr	FF	RST 7
29	DAD H	54	MOV D,H	7F	MOV A,A	AA	XRA D	D5	PUSH D		
2A	LHLD Adr	55	MOV D,L	80	ADD B	AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity. D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. Adr = 16-bit address.