2507/302
MICROCONTROLLER
TECHNOLOGY
Oct./Nov. 2017
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING
(AVIONICS OPTION)
MODULE III

MICROCONTROLLER TECHNOLOGY

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:
Answer booklet;
Non-programmable scientific calculator;
8051 Instruction set.
*Answer any **FIVE** of the **EIGHT** questions in the answer booklet provided.*
All questions carry equal marks.
Maximum marks for each part of a question are as indicated.
Candidates should answer the questions in English.

This paper consists of 6 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

1. (a) (i) State **four** advantages of a microcontroller over a microprocessor system. (4 marks)

(ii) Distinguish between Vonneumann and Harvard computer architectures. (4 marks)

(b) Draw a block diagram of a microcontroller and explain the process of start-up. (8 marks)

(c) Convert the following into decimal:

(i) $(1.011)_2$
(ii) $(3.14)_8$.

(4 marks)

2. (a) State **two** benefits of using programmable logic controller systems. (2 marks)

(b) With the aid of a block diagram, explain the functions of the various parts of a PLC system. (10 marks)

(c) A signal lamp is to be switched ON if a pump is running and the pressure is satisfactory, or if the lamp test switch is closed.

(i) Design a ladder logic diagram to represent the above condition.

(ii) Write a program list to realize c (i).

(8 marks)

3. (a) Explain the functions of the following 8051 flags:-

(i) carry (c);
(ii) overflow (0 V).

(4 marks)

(b) An 8051 is operating off a 12 MHz crystal.

(i) For a time delay of 1 msec, determine the value of the 16-bit timer register.

(ii) Write an assembly language subroutine to generate the delay of 1 msec. (10 marks)

(c) (i) Differentiate between MNEMONIC and OPERAND.

(ii) Explain the following instructions:

(I) INC R_1;
(II) LJMP LAB5.

(6 marks)

4. (a) Differentiate the operational aspects of the T_{CON} and T_{MOD} timer special function registers. (4 marks)

(b) Explain the mode 1 operation of the 8051 microcontroller internal timer registers. (7 marks)

(c) (i) Phase error occurs while reading the contents of Timer Registers. Explain how this can be avoided in an 8051 microcontroller based system. (4 marks)

(ii) Write an 8051 assembly language program to read the contents of timer registers TL_1/TH_1 into Registers R_6/R_7. (5 marks)

5. (a) (i) Define an 'interrupt' with respect to microcontrollers.

(ii) State **three** interrupt types in microcontrollers.

(4 marks)

(b) Draw the structure of the 8051 Interrupt Enable Special Function Register (SFR) and state the function of each bit. (8 marks)

(c) With the aid of a flow chart, explain the sequence of events that occur when an interrupt is detected by the 8051 microcontroller. (8 marks)

6. (a) Describe the following devices as applied to microcontrollers:

(i) relays;
(ii) opto-isolators.

(4 marks)

(b) A simple burglar alarm system has 4-Zone Inputs connected to Port 3 of 8051 I/O ports. If any one of these inputs is activated a buzzer will sound for 5 minutes and the corresponding zone LED or LEDs will be activated. The LEDs and the buzzer are connected to port 1.

(i) Draw a block schematic diagram for the system. (5 marks)

(ii) Write an 8051 assembly language program to implement the required functionality for the system described in b (i).
Assume 2.5 minutes delay subroutine, PRO-DELAY-SUB; is available.
(7 marks)

(c) A linear variable differential transformer is interfaced with a microcontroller to produce an rms output voltage 1 volt for a displacement of 200×10^{-6} mm.

Determine the sensitivity of the LVDT. (4 marks)

7. (a) With the aid of a circuit diagram, explain how a H-bridge is used to control a DC motor. (8 marks)

(b) With the aid of a block schematic diagram, explain how a stepper motor is controlled by a microcontroller through an electronic interface. (6 marks)

(c) Draw a flow chart of a program to rotate the motor in (b). (6 marks)

8. (a) With the aid of a diagram, explain the operation of a 3-bit flash ADC. (8 marks)

(b) Draw a schematic block diagram showing the interconnection of the following devices connected to an 8051 microcontroller system:

(i) potentiometer;
(ii) LM 35 Temperature sensor;
(iii) ADC/DAC;
(iv) 8051 microcontroller;
(v) amplifier and loudspeaker;
(vi) a 4-20 mA output terminal.

(6 marks)

(c) State:

(i) **four** merits of digital input/outputs in microcontroller based system;

(ii) **two** components of a SCADA system.

(6 marks)

Appendix A: Instruction Set of 8051 Microcontroller

Mnemonics, Arranged Alphabetically

MNEMONIC	DESCRIPTION	BYTES	CYCLES	FLAGS
ACALL addr11	PC + 2 → (SP); addr11 → PC	2	2	
ADD A, direct	A + (direct) → A	2	1	C OV AC
ADD A, @Ri	A + (Ri) → A	1	1	C OV AC
ADD A, #data	A + #data → A	2	1	C OV AC
ADD A, Rn	A + Rn → A	1	1	C OV AC
ADDC A, direct	A + (direct) + C → A	2	1	C OV AC
ADDC A, @Ri	A + (Ri) + C → A	1	1	C OV AC
ADDC A, #data	A + #data + C → A	2	1	C OV AC
ADDC A, Rn	A + Rn + C → A	1	1	C OV AC
AJMP addr11	Addr11 → PC	2	2	
ANL A, direct	A AND (direct) → A	2	1	
ANL A, @Ri	A AND (Ri) → A	1	1	
ANL A, #data	A AND #data → A	2	1	
ANL A, Rn	A AND Rn → A	1	1	
ANL direct, A	(direct) AND A → (direct)	2	1	
ANL direct, #data	(direct) AND #data → (direct)	3	2	
ANL C, bit	C AND bit → C	2	2	C
ANL C, $\overline{\text{bit}}$	C AND $\overline{\text{bit}}$ → C	2	2	C
CJNE A, direct, rel	[A <> (direct)]: PC + 3 + rel → PC	3	2	C
CJNE A, #data, rel	[A <> data]: PC + 3 + rel → PC	3	2	C
CJNE @Ri, #data, rel	[(Ri) <> data]: PC + 3 + rel → PC	3	2	C
CJNE Rn, #data, rel	[Rn <> data]: PC + 3 + rel → PC	3	2	C
CLR A	0 → A	1	1	
CLR bit	0 → bit	2	1	
CLR C	0 → C	1	1	0
CPL A	$\overline{\text{A}}$ → A	1	1	
CPL bit	$\overline{\text{bit}}$ → bit	2	1	
CPL C	$\overline{\text{C}}$ → C	1	1	C
DA A	Abin → Adec	1	1	C
DEC A	A – 1 → A	1	1	
DEC direct	(direct) – 1 → (direct)	2	1	
DEC @Ri	(Ri) – 1 →(Ri)	1	1	
DEC Rn	Rn – 1 → Rn	1	1	
DIV AB	A/B → AB	1	4	0 OV
DJNZ direct, rel	[(direct) – 1 <> 00]: PC + 3 + rel → PC	3	2	
DJNZ Rn, rel	[Rn – 1 <> 00]: PC + 2 + rel → PC	2	2	
INC A	A + 1 → A	1	1	
INC direct	(direct) + 1 → (direct)	2	1	
INC DPTR	DPTR + 1 → DPTR	1	2	
INC @Ri	(Ri) + 1 → (Ri)	1	1	
INC Rn	Rn + 1→ Rn	1	1	
JB bit, rel	[b=1]: PC + 3 + rel → PC	3	2	
JBC bit, rel	[b=1]: PC + 3 + rel → PC; 0 → bit	3	2	
JC rel	[C=1]: PC + 2 + rel → PC	2	2	
JMP @A + DPTR	DPTR + A → PC	1	2	
JNB bit, rel	[b=0]: PC + 3 + rel → PC	3	2	
JNC rel	[C=0]: PC + 2 + rel → PC	2	2	
JNZ rel	[A>00]: PC + 2 + rel → PC	2	2	
JZ rel	[A=00]: PC + 2 + rel → PC	2	2	
LCALL addr16	PC + 3 → (SP); addr16 → PC	3	2	
LJMP addr16	Addr16 → PC	3	2	
MOV A, direct	(direct) → A	2	1	
MOV A, @Ri	(Ri) → A	1	1	
MOV A, #data	#data → A	2	1	
MOV A, Rn	Rn → A	1	1	
MOV direct, A	A → (direct)	2	1	
MOV direct, direct	(direct) → (direct)	3	2	
MOV direct, @Ri	(Ri) → (direct)	2	2	
MOV direct, #data	#data → (direct)	3	2	
MOV direct, Rn	Rn → (direct)	2	2	
MOV bit, C	C → bit	2	2	C
MOV C, bit	bit → C	2	1	
MOV @Ri, A	A → (Ri)	1	1	
MOV @Ri, direct	(direct) → (Ri)	2	2	