2207/304
DIGITAL PRINCIPLES AND
MICROPROCESSORS
Oct./Nov. 2017
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING AVIONICS (COMMUNICATION AND NAVIGATION OPTION)

DIGITAL PRINCIPLES AND MICROPROCESSORS

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:
Answer booklet;
Non-programmable scientific calculator;
Instruction set (Intel 8080/8085).
*Answer any **FIVE** of the **EIGHT** questions in the answer booklet provided.*
All questions carry equal marks.
Maximum marks for each part of a question are as indicated.
Candidates should answer the questions in English.

This paper consists of 9 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

1. (a) Perform each of the following number conversions:

(i) $(6857.625)_{10}$ to octal;
(ii) $(4372.4051)_8$ to decimal;
(iii) $(26.85)_{10}$ to binary. (6 marks)

(b) Evaluate each of the following in the given bases:

(i)
$$\begin{array}{r} (7465)_8 \\ -(3577)_8 \\ \hline \end{array}$$

(ii)
$$\begin{array}{r} (FDE6)_{16} \\ +(3EFC)_{16} \\ \hline \end{array}$$

(iii) $(110111)_2 \div (101)_2$. (6 marks)

(c) (i) Convert the decimal number 3789 into:

I. 8 - 4 - 2 - 1 BCD;
II. Excess - 3;
III. ASCII; given that the ASCII code for 0 is 30 H.

(ii) Convert the binary number 101100 into gray code. (8 marks)

2. (a) Complete each of the following Boolean expressions, showing the proof in each case:

(i) $A + A + A =$
(ii) $\overline{A} + A\overline{B} =$ (6 marks)

(b) Simplify each of the following Boolean expressions:

(i) $(\overline{A} + B)(\overline{A} + C)$
(ii) $XYZ + X\overline{Y}Z + XY\overline{Z} + X\overline{Y}\,\overline{Z}$ (6 marks)

(c) (i) Define fan-in with respect to logic gates.

(ii) Figure 1 shows a circuit diagram of a digital gate.

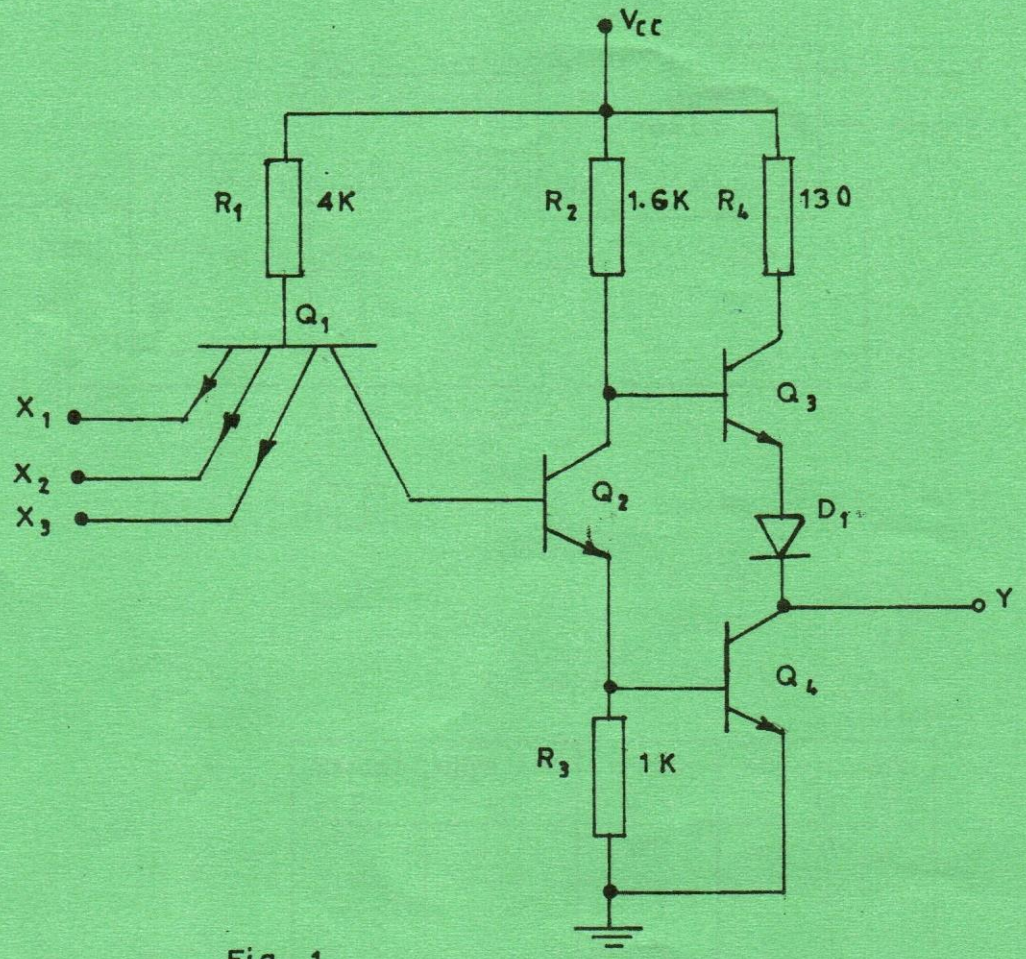

Fig. 1

I. state the gate's family.
II. explain the working of the gate.
III. with the aid of a truth table, derive the logic function implemented by the gate. (8 marks)

3. (a) (i) Draw the truth tables for each of the following flip-flops:

I. R-S;
II. T.

(ii) Draw a block schematic diagram showing how a T-flip flop could be obtained from a JK-flip flop. (10 marks)

(b) (i) Using D-flip flops, draw a block schematic diagram of a 4-bit serial-in serial-out (SISO) register.

(ii) Describe the operation of the register in b(i). (6 marks)

(c) Figure 2 shows a logic diagram of a sequential circuit. Complete its state transition in Table 1. (4 marks)

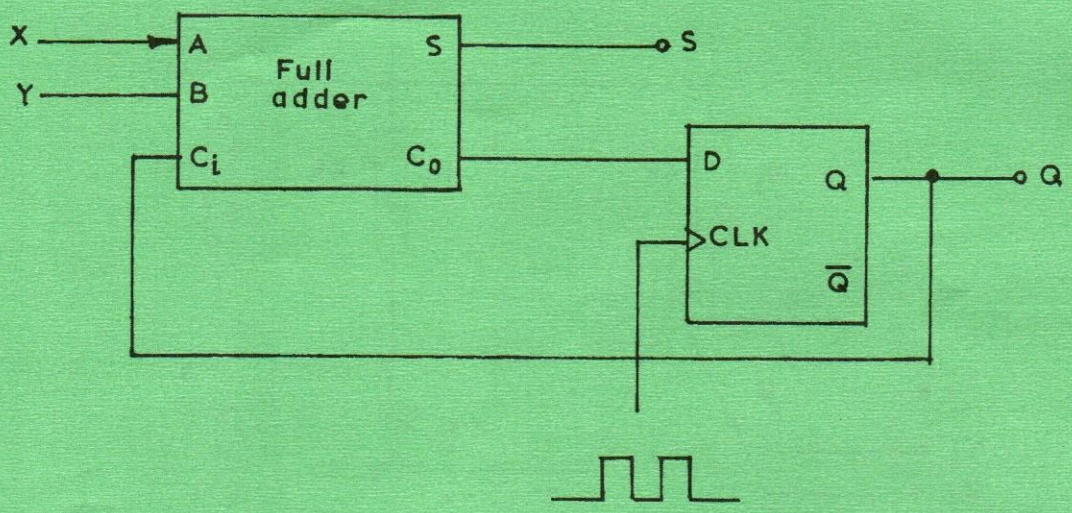

Fig. 2

Table 1

Present State Q	Inputs x, y	Next state Q+	Output S
0	0 0		
1	0 0		
0	0 1		
1	0 1		
0	1 0		
1	1 0		
0	1 1		
1	1 1		

4. (a) A combinational logic circuit has four inputs and one output. The output is equal to logic 1 when:

All inputs are equal to logic 1 or;
None of the inputs are equal to logic 1 or;
An odd number of inputs are equal to logic 1.

(i) Obtain the truth table for the circuit. (4 marks)

(ii) Using a K-map, obtain a simplified expression for the sum-of-Products (SOPs). (4 marks)

(iii) Draw a logic circuit diagram for the expression in a(ii) using NAND gates only. (4 marks)

(b) A combinational logic circuit is defined by the Boolean function, $F = \overline{X}YZ + X\overline{Y}Z$. Realize the circuit using:

(i) decoders and external gates only;
(ii) half adder logic circuits only. (8 marks)

5. (a) State **two** applications of digital counter. (2 marks)

(b) Figure 3 shows a state diagram of a 2-bit Gray Code Counter.

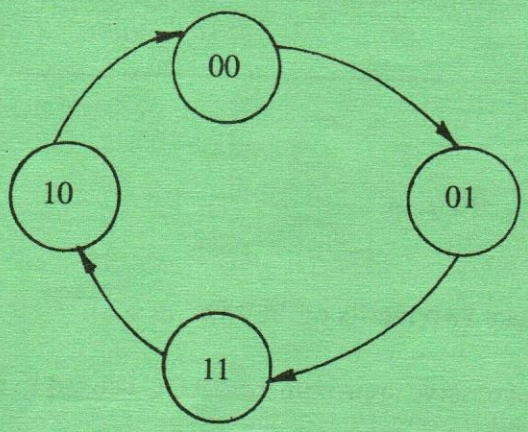

Fig. 3

(i) Draw a state transition table for the counter using JK-flip flops. (4 marks)

(ii) Using K-maps, derive minimized logic expressions for the JK inputs. (4 marks)

(iii) Draw the logic circuit diagram for the counter. (4 marks)

(c) (i) Draw a schematic logic diagram of a 4-bit Johnson counter.

(ii) Draw the truth table for the counter in c(i). (6 marks)

6. (a) (i) Define each of the following with respect to Anologue-to-Digital Converter (ADC);

I. resolution;
II. accuracy. (2 marks)

(ii) Figure 4 shows a schematic block diagram of an ADC. Describe its operation.

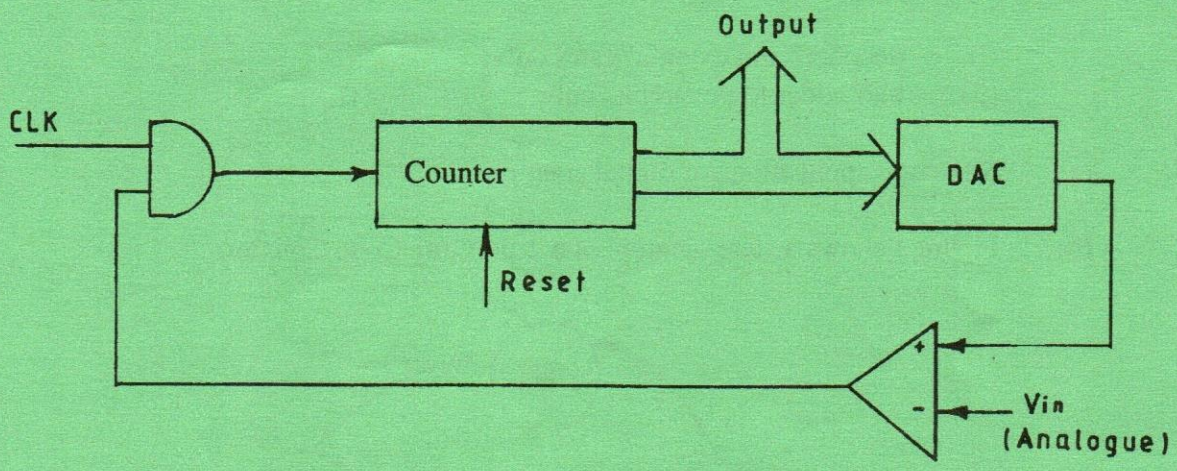

Fig. 4

(iii) State **two** merits of the ADC in a(ii). (7 marks)

(b) A 6-bit successive approximation ADC is used to convert an analogue signal. Determine its:

(i) percentage resolution;
(ii) time to convert a half-scale analogue signal if its clock frequency in 1MHz. (5 marks)

(c) Describe each of the following input/output techniques, stating one merit of each:

(i) polled;
(ii) interrupt. (6 marks)

7. (a) Define each of the following microprocessor addressing modes, illustrating each with an example:

(i) immediate;
(ii) relative;
(iii) absolute. (6 marks)

(b) Write an assembly language program to perform the following sequentially:

Subtract the decimal numbers, 96 - 17;
Multiply the result by 2;
Store the result in memory location 1806 H;
End. (5 marks)

(c) Table 2 shows an 8085 assembly language program.

Table 2

MV1 A, 20 H
MV1 B, 3C H
ADD B
ADD B
HLT

(i) With the aid of a trace table, determine the data in the accumulator at the end of the program execution.

(ii) Convert the program into 8085 hexadecimal machine code. (9 marks)

8. (a) A microcomputer has a 16 K X 8 - bit RAM which is made from 4K X 4 RAM chips.

(i) Determine the number of 4K X4 RAM chips needed;
(ii) Draw a block schematic diagram to show the memory implementation.

(6 marks)

(b) Figure 5 shows a circuit diagram of a temperature controller. The circuit compares the outside and the inside temperatures, then turns on a cooling fan when conditions are right.

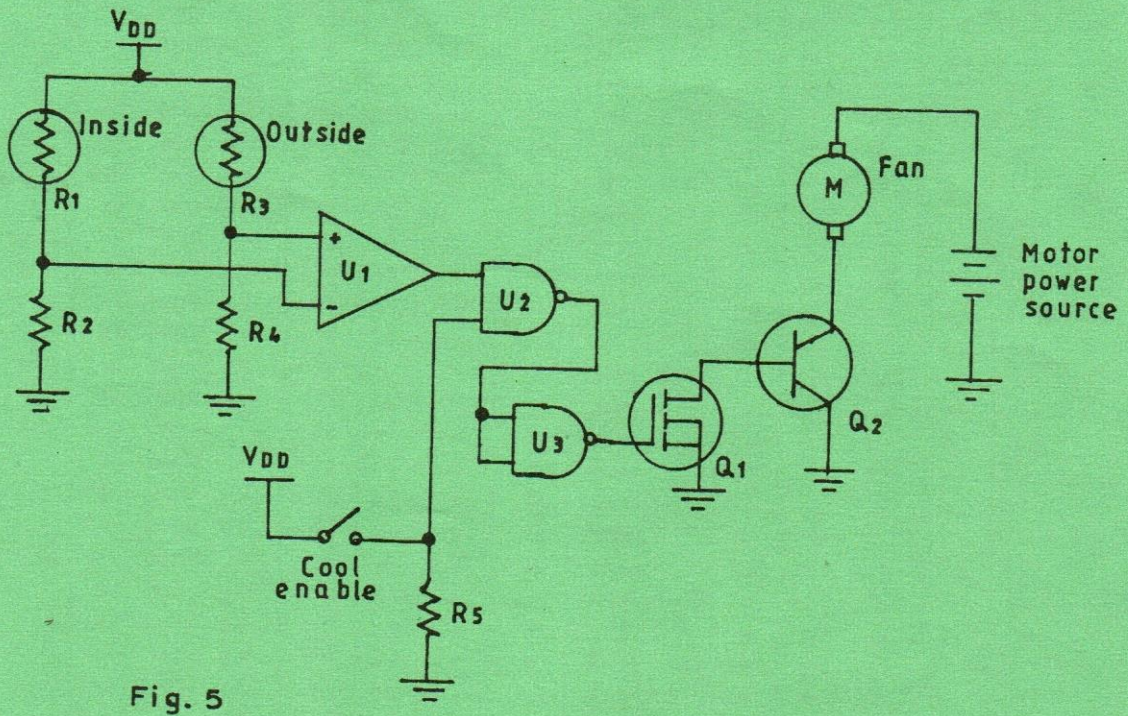

Fig. 5

Explain how the operation of the circuit will be affected by each of the following independent faults:

(i) NAND gate U_2 output is stack at logic O;
(ii) Transistor Q_1 drain-to-source is short circuited;
(iii) Resistor R_2 is open circuited;
(iv) Thermistor R_3 is open circuited. (8 marks)

(c) (i) Describe the checksum method of testing a microcomputer ROM memory.

(ii) Explain the drawback of the method in c(i). (6 marks)

Instruction set of

8080/8085

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	2B	DCX H	56	MOV D,M	81	ADD C	AC	XRA H	D7	RST 2
01	LX1 B,D16	2C	INR L	57	MOV D,A	82	ADD D	AD	XRA L	D8	RC
02	STAX B	2D	DCR L	58	MOV E,B	83	ADD E	AE	XRA M	D9	–
03	INX B	2E	MVI L,D8	59	MOV E,C	84	ADD H	AF	XRA A	DA	JC Adr
04	INR B	2F	CMA	5A	MOV E,D	85	ADD L	B0	ORA B	DB	IN D8
05	DCR B	30	SIM	5B	MOV E,E	86	ADD M	B1	ORA C	DC	CC Adr
06	MVI B,D8	31	LXI SPD16	5C	MOV E,H	87	ADD A	B2	ORA D	DD	–
07	RLC	32	STA Adr	5D	MOV E,L	88	ADC B	B3	ORA E	DE	SBI D8
08	–	33	INX SP	5E	MOV E,M	89	ADC C	B4	ORA H	DF	RST 3
09	DAD B	34	INR M	5F	MOV E,A	8A	ADC D	B5	ORA L	E0	RPO
0A	LDAX B	35	DCR M	60	MOV H,B	8B	ADC E	B6	ORA M	E1	POP H
0B	DCX B	36	MVI M,D8	61	MOV H,C	8C	ADC H	B7	ORA A	E2	JPO Adr
0C	INR C	37	STC	62	MOV H,D	8D	ADC L	B8	CMP B	E3	XTHL
0D	DCR C	38	–	63	MOV H,E	8E	ADC M	B9	CMP C	E4	CPO Adr
0E	MVI C,D8	39	DAD SP	64	MOV H,H	8F	ADC A	BA	CMP D	E5	PUSH H
0F	RRC	3A	LDA Adr	65	MOV H,L	8G	SUB B	BB	CMP E	E6	ANI D8
10	–	3B	DCX SP	66	MOV H,M	91	SUB C	BC	CMP H	E7	RST 4
11	LXI D,D16	3C	INR A	67	MOV H,A	92	SUB D	BD	CMP L	E8	RPE
12	STAX D	3D	DCR A	68	MOV L,B	93	SUB E	BE	CMP M	E9	PCHL
13	INX D	3E	MVI A,D8	69	MOV L,C	94	SUB H	BF	CMP A	EA	JPE Adr
14	INR D	3F	CMC	6A	MOV L,D	95	SUB L	C0	RNZ	EB	XCHG
15	DCR D	40	MOV B,B	6B	MOV L,E	96	SUB M	C1	POP B	EC	CPE Adr
16	MVI D,D8	41	MOV B,C	6C	MOV L,H	97	SUB A	C2	JNZ Adr	ED	–
17	RAL	42	MOV B,D	6D	MOV L,L	98	SBB B	C3	JMP Adr	EE	ERI D8
18	–	43	MOV B,E	6E	MOV L,M	99	SBB C	C4	CNZ Adr	EF	RST 5
19	DAD D	44	MOV B,H	6F	MOV L,A	9A	SBB D	C5	PUSH B	F0	RP
1A	LDAX D	45	MOV B,L	70	MOV M,B	9B	SBB E	C6	ADI D8	F1	POP PSW
1B	DCX D	46	MOV B,M	71	MOV M,C	9C	SBB H	C7	RST 0	F2	JP Adr
1C	INR E	47	MOV B,A	72	MOV M,D	9D	SBB L	C8	RZ	F3	DI
1D	DRC E	48	MOV C,B	73	MOV M,E	9E	SBB M	C9	RET Adr	F4	CP Adr
1E	MVI E,D8	49	MOV C,C	74	MOV M,H	9F	SBB A	CA	JZ	F5	PUSH PSW
1F	RAR	4A	MOV C,D	75	MOV M,L	A0	ANA B	CB	–	F6	ORI D8
20	RIM	4B	MOV C,E	76	HLT	A1	ANA C	CC	CZ Adr	F7	RST 6
21	LXI H,D16	4C	MOV C,H	77	MOV M,A	A2	ANA D	CD	CALL Adr	F8	RM
22	SHLD Adr	4D	MOV C,L	78	MOV A,B	A3	ANA E	CE	ACI D8	F9	SPHL
23	INX H	4E	MOV C,M	79	MOV A,C	A4	ANA H	CF	RST 1	FA	JM Adr
24	INR H	4F	MOV C,A	7A	MOV A,D	A5	ANA L	D0	RNC	FB	E1
25	DCR H	50	MOV D,B	7B	MOV A,E	A6	ANA M	D1	POP D	FC	CM Adr
26	MVI H,D8	51	MOV D,C	7C	MOV A,H	A7	ANA A	D2	JNC Adr	FD	–
27	DAA	52	MOV D,D	7D	MOV A,L	A8	XRA B	D3	OUT D8	FE	CPI D8
28	–	53	MOV D,E	7E	MOV A,M	A9	XRA C	D4	CNC Adr	FF	RST 7
29	DAD H	54	MOV D,H	7F	MOV A,A	AA	XRA D	D5	PUSH D		
2A	LHLD Adr	55	MOV D,L	80	ADD B	AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity. D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. Adr = 16-bit address.

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