2207/304
DIGITAL PRINCIPLES
AND MICROPROCESSORS
Oct./Nov. 2016
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING (AVIONICS) (COMMUNICATION AND NAVIGATION OPTION)

DIGITAL PRINCIPLES AND MICROPROCESSORS

3 hours

INSTRUCTIONS TO CANDIDATES

You should have a scientific calculator for this examination.
*Answer any **FIVE** of the **EIGHT** questions in the answer booklet provided.*
All questions carry equal marks.
Maximum marks for each part of a question are as shown.
Candidates should answer the questions in English.

This paper consists of 6 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

Turn over

1. (a) Perform each of the following number conversions:

(i) $(1101011)_2$ into octal form;

(ii) $(723.1275)_{10}$ into binary form;

(iii) $(EF2.B9)_{16}$ into binary form.

(7 marks)

(b) Calculate each of the following in the given bases:

(i) $(A94D)_{16}$
$+ (E3BF)_{16}$

(ii) $(5674)_8$
$- (2745)_8$

(iii) $(1101101)_2$
$\times (111011)_2$

(7 marks)

(c) Express the decimal number 8734 into:

(i) BCD;
(ii) excess -3 code;
(iii) ASC11.
NB: The ASCII code for 0 to be 30 H

(6 marks)

2. (a) (i) Distinguish between positive and negative logic.

(ii) Simplify the following using Boolean algebra:

(I) $(A+B)(A+C)$;
(II) $ABC + A\overline{B}C + AB\overline{C} + A\overline{B}\,\overline{C}$

(iii) Convert $B(A+\overline{C})$ into canonical form.

(9 marks)

(b) Table 1 shows a truth table for a logic function.

(i) Write down the output as:

(I) sums of products;
(II) product of sums.

(ii) With the aid of a K-map, obtain a simplified function of the output.

(iii) Obtain the logic circuit diagram for the function of a(ii) using NAND gates only.
(11 marks)

Table 1

Inputs			Outputs
x	y	z	f
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3. (a) With the aid of a block schematic diagram explain the operation of a master-slave JK-flip flop. (7 marks)

(b) (i) Draw the truth table of RS-flip flop and state its transition equation.

(ii) Draw a schematic block diagram, to show how a JK-flip flop is derived from an RS-flip flop and draw its truth table.
(7 marks)

(c) (i) Draw the binary counting sequence for a decade counter.

(ii) Determine the number of flip-flops used to implement the counter in c(i).

(iii) Implement the counter in c(i) using JK-flip flops.
(6 marks)

4. (a) (i) With the aid of a logic diagram explain the operation of a 4-bit parallel-in serial-out (PISO) shift register made from D-flip flops.

(ii) State **one** application of the register in a(i).
(8 marks)

$V_{out} = \frac{H_{code}}{2^n} \times V_{ref}$

$full\ scale = \frac{2^{n-1}}{2^n} \times V_{ref}$

ATIF R2

(b) A counter has a single 1-bit control input C. When C = 0, the 2-bit counter sequences through the binary code. When C = 1, it sequences through the gray code; as follows

Binary code: $00 \rightarrow 01 \rightarrow 11 \rightarrow 00 \rightarrow ...$
Gray code: $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 ...$

(i) Draw a state diagram for the counter labelling the states by their 2-bit codes and show the transitions to the next states for each value of C.

(ii) Draw a transition table for the counter in b(i) using JK-flip flop.

(iii) Using K-map, derive minimised equations for the counter.

(12 marks)

5. (a) (i) Draw a truth table of a binary full subtractor.

(ii) Using a 4-to-1 multiplexer, implement the subtractor in a(i).

(10 marks)

(b) (i) Draw a truth table for a 3-bit even parity generator.

(ii) Implement the circuit in b(i) using 3-to-8 decoder and OR-gate.

(6 marks)

(c) A 4-bit adder implements an excess-3 to BCD code conversion. Draw the block schematic diagram to show the circuit interconnection. (4 marks)

6. (a) Define each of the following with respect to digital-to-analog converter (DAC):

(i) resolution;
(ii) range.

(2 marks)

(b) (i) Draw a labelled block schematic diagram of a successive approximation analogue-to-digital converter (ADC) and describe its operation.

(ii) State **one** advantage and **one** disadvantage of the ADC in b(i) compared to a counter based ADC.

(9 marks)

(c) A 12-bit ADC is used to convert an analogue signal to digital form. Determine for the ADC, the:

(i) percentage resolution;

(ii) time taken to convert a half-scale analogue signal using a 2 MHz clock frequency if the ADC is:

(I) counter based;
(II) successive approximation.

(9 marks)

7. (a) Define each of the following with respect to memory devices:

(i) access time;
(ii) volatile.

(2 marks)

(b) A semi-conductor RAM whose capacity is 16 Kx8 is implemented using 4 Kx8 RAM chips. Determine for the 4 Kx8 chips the:

(i) number of chips required;
(ii) number of address lines.
(iii) draw a labelled block schematic diagram for the memory implementation.

(10 marks)

(c) With the aid of sketches, describe the storage and retrieval of data in a ferrite core memory cell.

(8 marks)

8. (a) Define each of the following microprocessor addressing modes; stating an example in each case:

(i) register;
(ii) immediate;
(iii) direct.

(6 marks)

(b) Write an assembly language program segment to perform the following sequence:

add the BCD number 54H and 37H
perform BCD correction
multiply the result by 2
store the answer in memory location 1802H
end.

(6 marks)

(c) (i) List any **two** types of faults that occur in digital gates.

(ii) With the aid of a labelled diagram, describe how to test a NOR gate using alogic probe and a pulser.

(8 marks)

Instruction set of

8080/8085

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	2B	DCX H	56	MOV D,M	81	ADD C	AC	XRA H	D7	RST 2
01	LX1 B,D16	2C	INR L	57	MOV D,A	82	ADD D	AD	XRA L	D8	RC
02	STAX B	2D	DCR L	58	MOV E,B	83	ADD E	AE	XRA M	D9	–
03	INX B	2E	MVI L,D8	59	MOV E,C	84	ADD H	AF	XRA A	DA	JC Adr
04	INR B	2F	CMA	5A	MOV E,D	85	ADD L	B0	ORA B	DB	IN D8
05	DCR B	30	SIM	5B	MOV E,E	86	ADD M	B1	ORA C	DC	CC Adr
06	MVI B,D8	31	LXI SPD16	5C	MOV E,H	87	ADD A	B2	ORA D	DD	–
07	RLC	32	STA Adr	5D	MOV E,L	88	ADC B	B3	ORA E	DE	SBI D8
08	–	33	INX SP	5E	MOV E,M	89	ADC C	B4	ORA H	DF	RST 3
09	DAD B	34	INR M	5F	MOV E,A	8A	ADC D	B5	ORA L	E0	RPO
0A	LDAX B	35	DCR M	60	MOV H,B	8B	ADC E	B6	ORA M	E1	POP H
0B	DCX B	36	MVI M,D8	61	MOV H,C	8C	ADC H	B7	ORA A	E2	JPO Adr
0C	INR C	37	STC	62	MOV H,D	8D	ADC L	B8	CMP B	E3	XTHL
0D	DCR C	38	–	63	MOV H,E	8E	ADC M	B9	CMP C	E4	CPO Adr
0E	MVI C,D8	39	DAD SP	64	MOV H,H	8F	ADC A	BA	CMP D	E5	PUSH H
0F	RRC	3A	LDA Adr	65	MOV H,L	8G	SUB B	BB	CMP E	E6	ANI D8
10	–	3B	DCX SP	66	MOV H,M	91	SUB C	BC	CMP H	E7	RST 4
11	LXI D,D16	3C	INR A	67	MOV H,A	92	SUB D	BD	CMP L	E8	RPE
12	STAX D	3D	DCR A	68	MOV L,B	93	SUB E	BE	CMP M	E9	PCHL
13	INX D	3E	MVI A,D8	69	MOV L,C	94	SUB H	BF	CMP A	EA	JPE Adr
14	INR D	3F	CMC	6A	MOV L,D	95	SUB L	C0	RNZ	EB	XCHG
15	DCR D	40	MOV B,B	6B	MOV L,E	96	SUB M	C1	POP B	EC	CPE Adr
16	MVI D,D8	41	MOV B,C	6C	MOV L,H	97	SUB A	C2	JNZ Adr	ED	–
17	RAL	42	MOV B,D	6D	MOV L,L	98	SBB B	C3	JMP Adr	EE	ERI D8
18	–	43	MOV B,E	6E	MOV L,M	99	SBB C	C4	CNZ Adr	EF	RST 5
19	DAD D	44	MOV B,H	6F	MOV L,A	9A	SBB D	C5	PUSH B	F0	RP
1A	LDAX D	45	MOV B,L	70	MOV M,B	9B	SBB E	C6	ADI D8	F1	POP PSW
1B	DCX D	46	MOV B,M	71	MOV M,C	9C	SBB H	C7	RST 0	F2	JP Adr
1C	INR E	47	MOV B,A	72	MOV M,D	9D	SBB L	C8	RZ	F3	DI
1D	DRC E	48	MOV C,B	73	MOV M,E	9E	SBB M	C9	RET Adr	F4	CP Adr
1E	MVI E,D8	49	MOV C,C	74	MOV M,H	9F	SBB A	CA	JZ	F5	PUSH PSW
1F	RAR	4A	MOV C,D	75	MOV M,L	A0	ANA B	CB	–	F6	ORI D8
20	RIM	4B	MOV C,E	76	HLT	A1	ANA C	CC	CZ Adr	F7	RST 6
21	LXI H,D16	4C	MOV C,H	77	MOV M,A	A2	ANA D	CD	CALL Adr	F8	RM
22	SHLD Adr	4D	MOV C,L	78	MOV A,B	A3	ANA E	CE	ACI D8	F9	SPHL
23	INX H	4E	MOV C,M	79	MOV A,C	A4	ANA H	CF	RST 1	FA	JM Adr
24	INR H	4F	MOV C,A	7A	MOV A,D	A5	ANA L	D0	RNC	FB	EI
25	DCR H	50	MOV D,B	7B	MOV A,E	A6	ANA M	D1	POP D	FC	CM Adr
26	MVI H,D8	51	MOV D,C	7C	MOV A,H	A7	ANA A	D2	JNC Adr	FD	–
27	DAA	52	MOV D,D	7D	MOV A,L	A8	XRA B	D3	OUT D8	FE	CPI D8
28	–	53	MOV D,E	7E	MOV A,M	A9	XRA C	D4	CNC Adr	FF	RST 7
29	DAD H	54	MOV D,H	7F	MOV A,A	AA	XRA D	D5	PUSH D		
2A	LHLD Adr	55	MOV D,L	80	ADD B	AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity. D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. Adr = 16-bit address.

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