2207/304
DIGITAL PRINCIPLES AND MICROPROCESSORS
Oct./ Nov. 2011
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING AVIONICS (COMMUNICATION AND NAVIGATION OPTION)

DIGITAL PRINCIPLES AND MICROPROCESSORS

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:

Answer booklet;
Electronic Calculator;
Intel 8085 instruction set.

*Answer any **FIVE** of the **EIGHT** questions in this paper.*
***ALL** questions carry equal marks.*
Maximum marks for each part of a question are as shown.

This paper consists of 7 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

1. (a) Determine the decimal value of the 8-bit binary number 1000 0101 if it is read as a:

(i) unsigned number;

(ii) 2's complement signed number;

(iii) 8-4-2-1 BCD number. (8 marks)

(b) Convert the number 976_{10} to a:

(i) hexadecimal number;

(ii) binary number;

(iii) octal number. (6 marks)

(c) Use 8-bit 2's complement arithmetic to evaluate $(-37)_{10} - (69)_{10}$. (6 marks)

2. (a) (i) Using Boolean algebra show that:

$$AB + \bar{A}C + BC = AB + \bar{A}C.$$

(ii) Simplify the following expression using Boolean algebra:

$$\overline{AB + AC} + \bar{A} \cdot \bar{B} \cdot C$$

(iii) Express $\overline{A + B} + C$ in canonical sum-of-product (SOP) expression form. (9 marks)

(b) Using a K-map determine the minimal SOP expression for:

$$F(A,B,C,D) = \Sigma(0,2,4,6,7,10,13,14,15)$$ (6 marks)

(c) For the circuit of figure 1, draw the truth table; hence write the canonical SOP expression for Z. (5 marks)

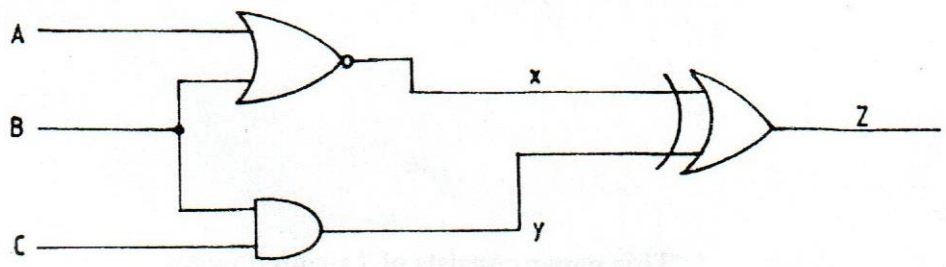

Fig. 1

3. (a) (i) Distinguish between 'astable' and 'bistable' with respect to multivibrators.

(ii) The waveforms for signals A and B shown in figure 2(a) are applied to the circuit of figure 2(b). Draw the waveforms for R, S, Q and $\overline{Q}$. Assume the following initial conditions; Q = O and $\overline{Q}$ = 1. (8 marks)

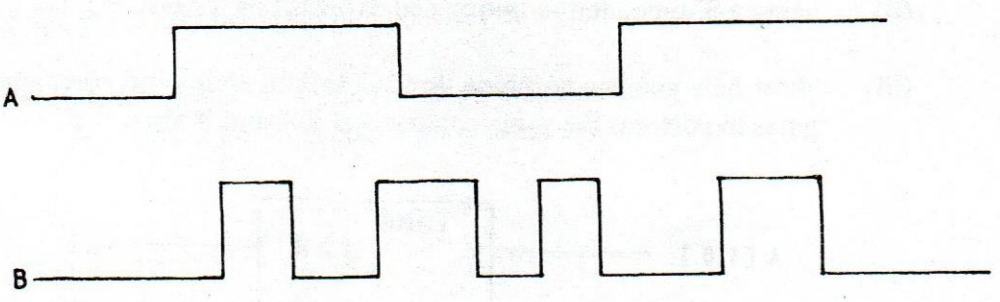

Fig. 2 (a)

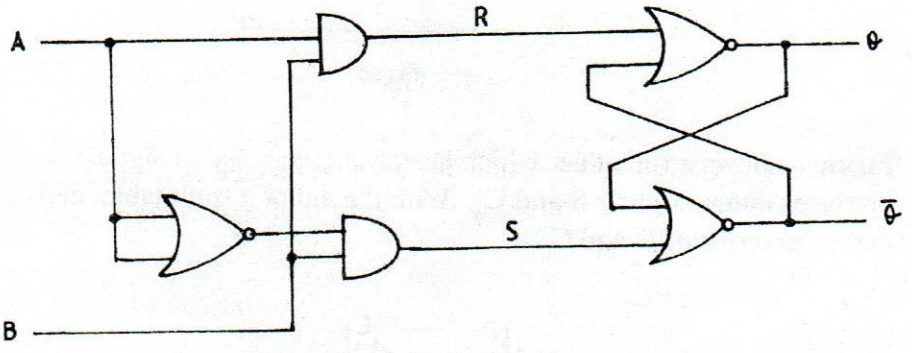

Fig. 2 (b)

(b) (i) Draw the truth table of a J-K flip-flop.

(ii) Show how a D flip-flop is derived from the table in b(i) and sketch its schematic diagram. (5 marks)

(c) For a divide-by-eight negative-edge triggered synchronous J-K counter, sketch the:

(i) logic diagram;

(ii) output waveforms for each stage of the counter with respect to the input clock pulses. (7 marks)

4. (a) Figure 3 shows an arithmetic module, COMP, that performs comparison between two 2-bit unsigned numbers A[1:0] and B[1:0]. It produces a logic '1' on output GT, EQ and LT if A>B, A=B and A<B respectively:

(i) draw the truth table for the module;

(ii) using a K-map, derive minimised expressions for GT, EQ and LT;

(iii) show how you can combine three COMP modules and other appropriate logic gates to perform the same comparison if A and B are 4-bits. (16 marks)

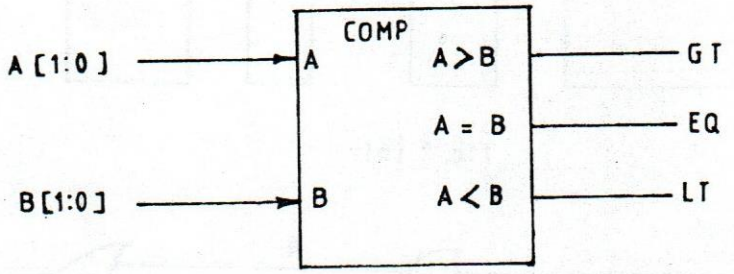

Fig.3

(b) Figure 4 shows a full adder which has been connected to signals D and C_i and produces output signals S and C_o. With the aid of a truth table, derive expressions for S and C_o in terms of D and C_i. (4 marks)

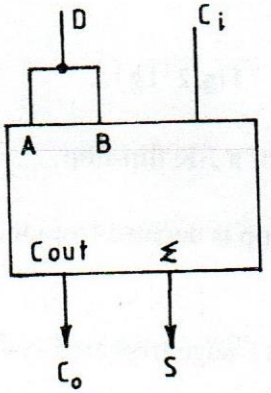

Fig. 4

5. (a) (i) With the aid of a block schematic diagram, explain the operation of a master-slave JK flip-flop.

(ii) Explain why a master-slave configuration is preferred to a standard JK flip-flop. (10 marks)

(b) With the aid of a logic diagram, describe the operation of a 4-bit right/ left shift register made from D-flip-flops and appropriate gates. (8 marks)

(c) State any **two** desired characteristics of a logic family. (2 marks)

6. (a) Define the following parameters with respect to digital-to-analogue converters:

(i) range;

(ii) resolution. (2 marks)

(b) (i) Draw a block diagram of a successive approximation analogue-to-digital converter (ADC) and describe its operation.

(ii) State **one** advantage and **one** disadvantage of the ADC in b(i). (9 marks)

(c) The voltage set to pin Vref of an 8-bit ADC chip is 4V. Determine the:

(i) ADC resolution;

(ii) digital value corresponding to a 3V analogue input voltage;

(iii) the maximum time taken to convert the signal using a 5 MHZ clock frequency if the ADC is:

I. counter based;

II. successive approximation. (9 marks)

7. (a) Draw a block diagram of a microprocessor-based system and state the function(s) of each part. (8 marks)

(b) (i) Define the following microprocessor addressing modes:

I. register;

II. inherent;

III. indirect.

(ii) Write an assembly language program segment to evaluate:

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(iii) Determine the hexadecimal machine code for the program in b(ii). (12 marks)

8. (a) Define the following with respect to computer memory access:

(i) serial;

(ii) random. (2 marks)

(b) A semiconductor RAM whose capacity is 32K x 8 is to be implemented using 8K x 4 RAM chips:

(i) determine the number of 8K x 4 RAM chips required;

(ii) draw a labelled block schematic diagram showing the memory implementation.

(10 marks)

(c) Figure 5 shows a microcomputer memory. The outputs of the decoding logic are as follows:

$CEA = (A15 + \overline{A14})$

$CEB = \overline{A_{15} \cdot A_{10} \cdot A_9}$

Determine the ranges of hexadecimal memory addresses to which each device responds.

(5 marks)

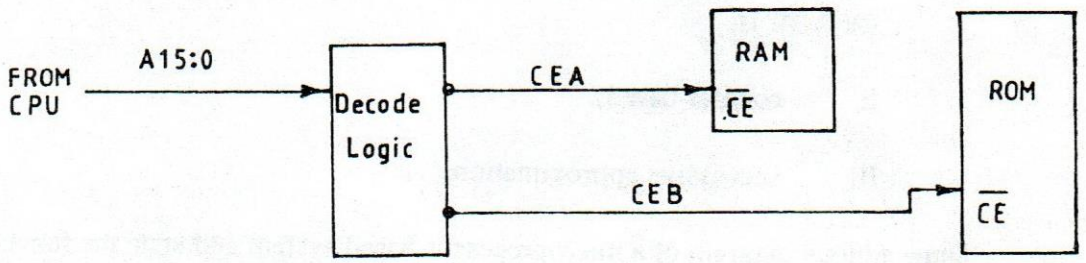

Fig. 5

(d) State the **three** principal input/output data transfer techniques. (3 marks)