2207/304
DIGITAL PRINCIPLES AND MICROPROCESSORS
Oct./Nov. 2009
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING AVIONICS

(COMMUNICATION AND NAVIGATION OPTION)

DIGITAL PRINCIPLES AND MICROPROCESSORS

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:

Answer booklet;
Electronic calculator.
Intel 8085 Instruction Set.

*Answer any **FIVE** of the **EIGHT** questions in this paper.*
All questions carry equal marks.

This paper consists of 7 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

1. (a) (i) Convert the following numbers into binary:

I. 15.75_{10}

II. 65.7_8 .

(ii) Evaluate the following; showing all the workings:

I. $BEBC_{16}$
$- 94EF_{16}$

II. 11011_2
$\times 11110_2$ (9 marks)

(b) (i) If the ASCII code for the letter A is 41H, deduce the ASCII codes for the word: **BOY**

(ii) For the one byte number, 10011101_2, determine its decimal value if it is in:

I. one's complement;
II. two's complement;
III. unsigned.

(iii) Convert the binary number, 110101, into Gray code. (11 marks)

2. (a) An Engine has four fail-safe sensors, S_1, S_2, S_3 and S_4. The engine should keep running unless any of the following conditions arise:

- if sensor S_2 is activated;
- if sensor S_1 and sensor S_3 are activated at the same time;
- if sensor S_3 and sensor S_4 are activated at the same time.

Take the output, F, to be logic '1' for engine running and the sensors to be at logic '1' for activation. For the system:

(i) derive the truth table for engine run;
(ii) with the aid of a K-map, derive a minimum logic expression for engine running;
(iii) implement the expression in a(ii) using NAND gates only. (12 marks)

(b) (i) Prove the following rule of boolean algebra:

$A + \bar{A}B = A + B$

(ii) For the circuit of Fig. 1:

I. derive the truth table; using positive logic;

II. derive the minimal binary logic expression. (8 marks)

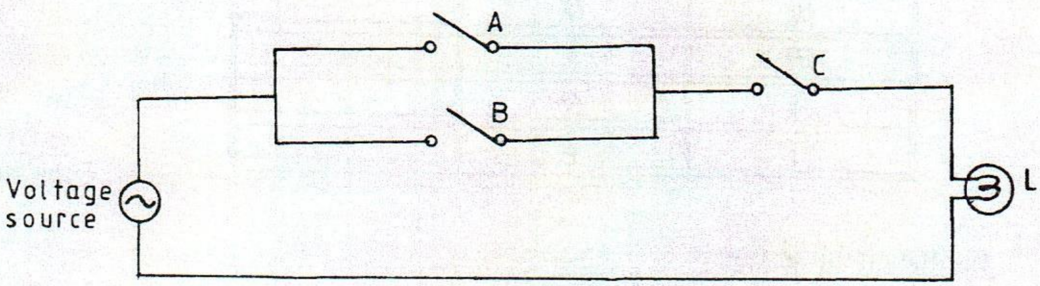

Figure 1

3. (a) For the R - S NOR circuit of Fig. 2:

(i) derive the expression for the next state, Q(t + 1), in terms of the present state, Q,and the inputs R and S;

(ii) complete table 1;

(iii) modify the circuit to form a JK flip flop. (10 marks)

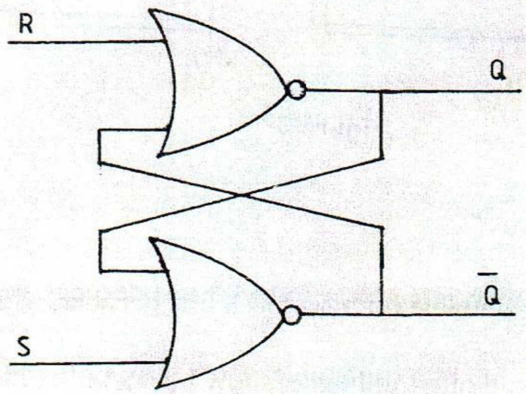

Figure 2

Table 2

RS	PRESENT STATE (Q)	NEXT STATE $(Q(t+1))$
00	0	
00	1	
01	0	
01	1	
10	0	
10	1	
11	0	
11	1	

3. (b) For the circuit of Fig. 3:

(i) draw the timing diagram for the outputs Q_0, Q_1, Q_2 and the input clock CLK, for at least nine (9) clock cycles;

(ii) derive the sequence of counts generated;

(iii) determine the frequency of Q_2, if the clock frequency is 40Hz;

(iv) state any **two** disadvantages. (10 marks)

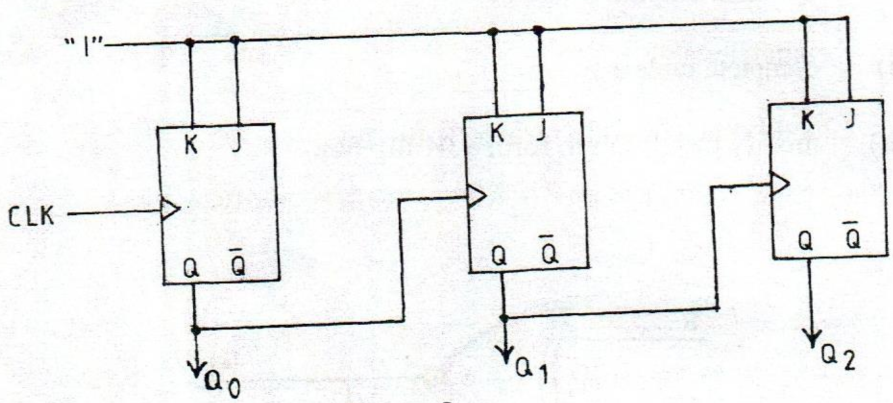

Figure 3

4. (a) (i) Draw a truth table for a 3 - to - 8 line decoder, with active high outputs.

(ii) With the aid of a truth table, show how a full -adder can be implemented by a 3- to - 8 decoder and OR - gates.

(iii) Draw the block schematic of the full-adder in a(ii). (12 marks)

(b) (i) With the aid of a logic diagram, explain the operation of D flip-flop based, 4-bit synchronous Johnson counter.

(ii) State the advantage of the counter in b(i). (8 marks)

5. (a) (i) Define the following with respect to a digital analogue converter (DAC):

I. off-set error;

II. sampling rate.

(ii) Draw a circuit diagram of a 4-bit, OP-AMP based, R - 2R DAC.

(iii) In a 4-bit binary weighted DAC, the resistor for the most significant Bit (MSB) has a value of 25 KΩ. Determine the:

I. values of the other input resistors;

II. feedback resistor, R_f, if the maximum output Voltage is -3.75V and the input reference Voltage is +5V.

(11 marks)

(b) A 10 bit Analogue to digital converter (ADC) is used to convert a half-scale analogue signal. Determine:

(i) the percentage signal resolution;

(ii) the time taken to convert the signal, using a 1MHz clock frequency, if the ADC is :

I. counter based;

II. successive approximation. (9 marks)

6. (a) Define the following with respect to memory devices:

(i) memory word;

(ii) access time;

(iii) volatile. (3 marks)

(b) A semiconductor RAM chip is specified as 8K x 16. Determine for the chip, the:

(i) number of address lines;

(ii) number of data lines;

(iii) memory capacity in Kilobytes. (5 marks)

(c) Answer TRUE or FALSE to each of the following statements:

(i) All semiconductor memories are non-volatile.

(ii) NMOS memory is a category of binary memory.

(iii) EPROMS can be programmed and erased several times.

(iv) All RAMs are volatile.

(v) SRAMs retain their stored data state as long as electric power is maintained.

(5 marks)

(d) With the aid of a circuit diagram, describe the operation of the MOS static RAM cell.

(7 marks)

7. (a) Draw a labelled block diagram of the internal architecture of an 8 - bit microprocessor and state the function(s) of each part. (8 mark)

(b) Define each of the following microprocessor addressing modes, illustrating each case with a one line instruction:
(i) immediate;
(ii) direct;
(iii) indexed. (6 marks)

(c) Write an assembly language program to perform the following:
- add, three 8-bit numbers, in consecutive memory locations, starting from location 3000H;
- complement the result;
- store the result in memory location 3008H. (6 marks)

8. (a) (i) List any **three** faults found in a digital system.
(ii) With the aid of a labelled diagram, describe how to test a NAND gate using a logic probe and a pulser. (10 marks)

(b) Fig. 4 is a block schematic diagram of a decade counter and its seven segment display. A short circuit has occurred on the counter output Q_c to ground.
(i) Draw the truth table for the decoder/driver, when operating correctly.
(ii) Determine the counter output, with the fault.
(iii) Deduce the displayed count sequence of the display in b(ii). (10 marks)

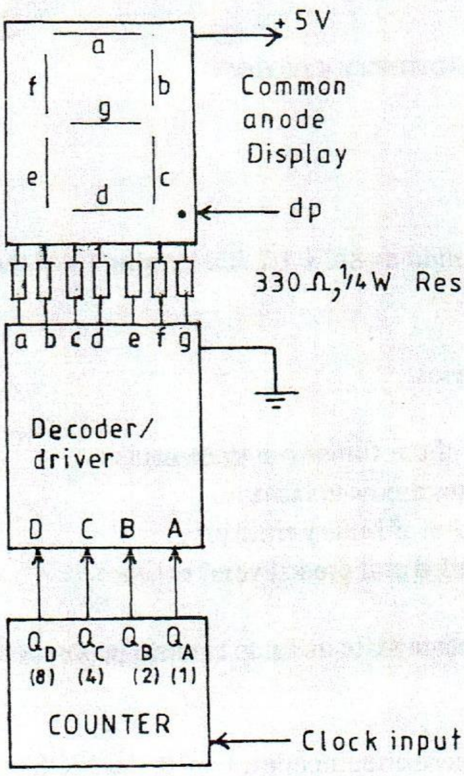

Figure 4

Instruction set of **8080/8085**

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	2B	DCX H	56	MOV D,M	81	ADD C	AC	XRA H	D7	RST 2
01	LX1 B,D16	2C	INR L	57	MOV D,A	82	ADD D	AD	XRA L	D8	RC
02	STAX B	2D	DCR L	58	MOV E,B	83	ADD E	AE	XRA M	D9	—
03	INX B	2E	MVI L,D8	59	MOV E,C	84	ADD H	AF	XRA A	DA	JC Adr
04	INR B	2F	CMA	5A	MOV E,D	85	ADD L	B0	ORA B	DB	IN D8
05	DCR B	30	SIM	5B	MOV E,E	86	ADD M	B1	ORA C	DC	CC Adr
06	MVI B,D8	31	LXI SPD16	5C	MOV E,H	87	ADD A	B2	ORA D	DD	—
07	RLC	32	STA Adr	5D	MOV E,L	88	ADC B	B3	ORA E	DE	SBI D8
08	—	33	INX SP	5E	MOV E,M	89	ADC C	B4	ORA H	DF	RST 3
09	DAD B	34	INR M	5F	MOV E,A	8A	ADC D	B5	ORA L	E0	RPO
0A	LDAX B	35	DCR M	60	MOV H,B	8B	ADC E	B6	ORA M	E1	POP H
0B	DCX B	36	MVI M,D8	61	MOV H,C	8C	ADC H	B7	ORA A	E2	JPO Adr
0C	INR C	37	STC	62	MOV H,D	8D	ADC L	B8	CMP B	E3	XTHL
0D	DCR C	38	——	63	MOV H,E	8E	ADC M	B9	CMP C	E4	CPO Adr
0E	MVI C,D8	39	DAD SP	64	MOV H,H	8F	ADC A	BA	CMP D	E5	PUSH H
0F	RRC	3A	LDA Adr	65	MOV H,L	8G	SUB B	BB	CMP E	E6	ANI D8
10	——	3B	DCX SP	66	MOV H,M	91	SUB C	BC	CMP H	E7	RST 4
11	LXI D,D16	3C	INR A	67	MOV H,A	92	SUB D	BD	CMP L	E8	RPE
12	STAX D	3D	DCR A	68	MOV L,B	93	SUB E	BE	CMP M	E9	PCHL
13	INX D	3E	MVI A,D8	69	MOV L,C	94	SUB H	BF	CMP A	EA	JPE Adr
14	INR D	3F	CMC	6A	MOV L,D	95	SUB L	C0	RNZ	EB	XCHG
15	DCR D	40	MOV B,B	6B	MOV L,E	96	SUB M	C1	POP B	EC	CPE Adr
16	MVI D,D8	41	MOV B,C	6C	MOV L,H	97	SUB A	C2	JNZ Adr	ED	——
17	RAL	42	MOV B,D	6D	MOV L,L	98	SBB B	C3	JMP Adr	EE	ERI D8
18	——	43	MOV B,E	6E	MOV L,M	99	SBB C	C4	CNZ Adr	EF	RST 5
19	DAD D	44	MOV B,H	6F	MOV L,A	9A	SBB D	C5	PUSH B	F0	RP
1A	LDAX D	45	MOV B,L	70	MOV M,B	9B	SBB E	C6	ADI D8	F1	POP PSW
1B	DCX D	46	MOV B,M	71	MOV M,C	9C	SBB H	C7	RST 0	F2	JP Adr
1C	INR E	47	MOV B,A	72	MOV M,D	9D	SBB L	C8	RZ	F3	DI
1D	DRC E	48	MOV C,B	73	MOV M,E	9E	SBB M	C9	RET Adr	F4	CP Adr
1E	MVI E,D8	49	MOV C,C	74	MOV M,H	9F	SBB A	CA	JZ	F5	PUSH PSW
1F	RAR	4A	MOV C,D	75	MOV M,L	A0	ANA B	CB	—	F6	ORI D8
20	RIM	4B	MOV C,E	76	HLT	A1	ANA C	CC	CZ Adr	F7	RST 6
21	LXI H,D16	4C	MOV C,H	77	MOV M,A	A2	ANA D	CD	CALL Adr	F8	RM
22	SHLD Adr	4D	MOV C,L	78	MOV A,B	A3	ANA E	CE	ACI D8	F9	SPHL
23	INX H	4E	MOV C,M	79	MOV A,C	A4	ANA H	CF	RST 1	FA	JM Adr
24	INR H	4F	MOV C,A	7A	MOV A,D	A5	ANA L	D0	RNC	FB	E1
25	DCR H	50	MOV D,B	7B	MOV A,E	A6	ANA M	D1	POP D	FC	CM Adr
26	MVI H,D8	51	MOV D,C	7C	MOV A,H	A7	ANA A	D2	JNC Adr	FD	——
27	DAA	52	MOV D,D	7D	MOV A,L	A8	XRA B	D3	OUT D8	FE	CPI D8
28	——	53	MOV D,E	7E	MOV A,M	A9	XRA C	D4	CNC Adr	FF	RST 7
29	DAD H	54	MOV D,H	7F	MOV A,A	AA	XRA D	D5	PUSH D		
2A	LHLD Adr	55	MOV D,L	80	ADD B	AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity. D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. Adr = 16-bit address.