2207/304
DIGITAL PRINCIPLES AND MICROPROCESSORS
Oct/Nov. 2004
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING AVIONICS (COMMUNICATIONS AND NAVIGATION OPTION)

DIGITAL PRINCIPLES AND MICROPROCESSORS

3 hours

INSTRUCTIONS TO CANDIDATES:

You should have the following for this examination:

Answer booklet
Mathematical table/calculator

Answer any **FIVE** of the following **EIGHT** questions.
All questions carry equal marks.

This paper consists of 5 printed pages

+2149320902

1. (a) Perform the following number conversions:

(i) 11011110.101_2 to decimal

(ii) 675.5_8 to binary

(4 marks)

(b) Add $5C4D_{16}$ to $3F9A_{16}$ and convert the results to binary. (4 marks)

(c) (i) Add:

I 384 to 596 in BCD (8421) code.

II 63 to 52 in excess - 3 code.

(ii) Evaluate:

(I) $1010_2 \times 1101_2$

(II) $110110 \div 101_2$

(12 marks)

2. (a) (i) State any TWO merits of a NAND gate over an AND gate.

(ii) Implement the express F = A + B using NAND gates only.

(5 marks)

(b) (i) Draw the logic circuit for the Boolean equation:

$$F = \overline{\overline{C.(A+B)+D}}$$

(ii) Using K' map, minimize the Boolean equation below as far as possible and hence draw the resultant logic gate:

$$A\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,B\,\overline{C}\,D + A\,B\,\overline{C}\,D + \overline{A}\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,C\,\overline{D} + \overline{A}\,\overline{B}\,C\,\overline{D} + \overline{A}BCD + ABCD$$

(6 marks)

(c) (i) With the aid of a logic circuit, describe the operation of a basic 2 - input TTL NAND gate.

(ii) Explain "propagation delay" as applied to logic intergrated circuits.

(9 marks)

(b) (i) Describe the operation of a signature analyser.

(ii) Draw a flow diagram for the program algorithm below:

Set the total to Zero
Repeat
Input a number
Add it to the total
Until a Zero input
Output the total.

(8 marks)

3. (a) (i) List any TWO applications of shift registers.

(ii) Draw a logic circuit of a 4 - bit serial - in parallel - out shift register using D- type flip - flops and describe its operation.

(8 marks)

(b) Explain the following as applied to digital counters:

(i) Synchronous

(ii) Asynchronous.

(4 marks)

(c) Draw the truth table and timing diagrams of a modulo - 6 ripple binary up - counter hence obtain the logic diagram.

(8 marks)

4. (a) (i) Define the following as applied to digital memories:

I Memory address

II Volatile memory

III Access memory.

(ii) With the aid of circuit diagram, describe the operation of a bipolar RAM memory cell.

(10 marks)

(b) (i) Draw a labelled memory map for a memory unit consisting of:

2K ROM 1 from location 0000_{16}

6K Spare from location 0800_{16}

2K ROM2 from location 2000_{16}

61K RAM from location 2800_{16}

(ii) A memory chip is configured as 16K x 16.

Determine:

I the number of address lines

II the total memory capacity

III the size of the data bus.

(10 marks)

5. (a) (i) Define the following as applied to digital signal converters:

I resolution

II monotonicity

(ii) With the aid of a labelled block diagram, describe the operation of a successive approximation analog-to-digital converter.

(9 marks)

(b) (i) With the aid of a circuit diagram, describe the operation of a 4 - bit binary - weighted resistor digital-to-analog converter.

(ii) An R/2R digital-to-analog converter is driven by the digital word 01111011_2. Determine the analog output voltage if the reference voltage is 9 volts.

(11 marks)

6. (a) (i) State any TWO applications of the output port in digital systems.

(ii) Explain "Software programmed" as applied to interfacing circuits.

(4 marks)

(b) For figure 1, explain the functions of the following pins:

(i) CS

(ii) Port B

(iii) A_0A_1

(6 marks)

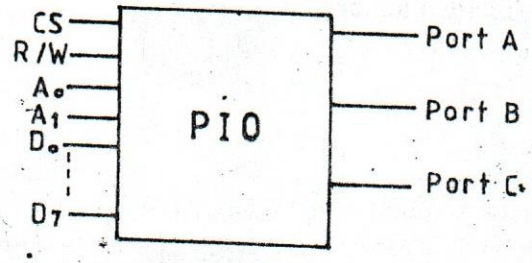

Fig. 1

(c) (i) Draw a labelled block diagram of an interrupt driven CPU with four peripheral and explain its operation.

(ii) Describe "Software polling" as applied to interfacing.

(10 marks)

7. (a) (i) List any TWO areas of applications of decoders in digital systems.

(ii) Draw the binary/octal decoder truth table and hence derive the logic circuit using AND gates.

(10 marks)

(b) (i) State, with reasons, the need for a parity checker circuit in digital systems.

(ii) Draw a logic circuit of a 4-bit parallel binary adder and describe its operation.

(10 marks)

8. (a) (i) Explain how "Direct Memory Access" is implemented in a microprocessor unit.

(ii) Draw a labelled block diagram of the internal organisation of the Central Processing Unit CPU) and state the function of each unit.

(12 marks)