

2521/203      2602/202  
2601/202      2603/202  
**DIGITAL AND ANALOGUE  
ELECTRONICS II**  
Oct./Nov. 2021  
Time: 3 hours



**THE KENYA NATIONAL EXAMINATIONS COUNCIL**  
**DIPLOMA IN ELECTRICAL AND ELECTRONICS ENGINEERING**  
**(POWER OPTION)**  
**(TELECOMMUNICATION OPTION)**  
**(INSTRUMENTATION OPTION)**

**MODULE II**

**DIGITAL AND ANALOGUE ELECTRONICS II**

**3 hours**

**INSTRUCTIONS TO CANDIDATES**

*You should have the following for this examination:*

*Answer booklet;*

*Drawing instruments;*

*Mathematical tables/non-programmable scientific calculator;*

*This paper consists of **EIGHT** questions in **TWO** sections, **A** and **B**.*

*Answer **TWO** questions from section **A**, and **THREE** questions from section **B** in the answer booklet provided.*

*All questions carry equal marks.*

*Maximum marks for each part of a question are as indicated.*

*Candidates should answer the questions in English.*

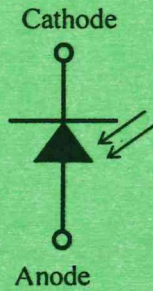
**This paper consists of 6 printed pages and one insert.**

**Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.**

## SECTION A: ANALOGUE ELECTRONICS II

Answer any **TWO** questions from this section.

1. (a) State **three** merits of light emitting diodes (LED). (3 marks)
- (b) **Figure 1** shows a symbol of an electronic device.

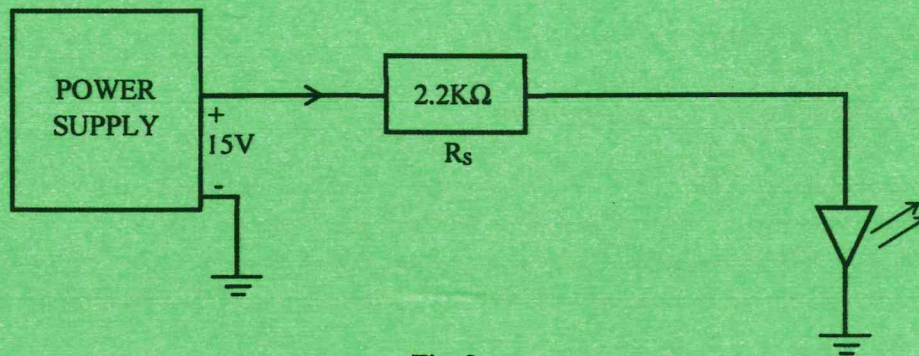


**Fig. 1**

- (i) identify the device;
- (ii) describe its principle of operation.

(6 marks)

- (c) **Figure 2** shows an electronic circuit. The voltage drop across the LED is 2 V.



**Fig. 2**

Determine the:

- (i) current through the LED;
- (ii) power dissipated at the resistor.

(4 marks)

- (d) A single stage amplifier has a voltage gain of 50. The collector load  $R_c$  is  $400\ \Omega$  and the input impedance is  $1\ \text{K}\Omega$ . If two such stages are cascaded through R - C coupling, determine the:
- (i) effective load of the first stage;
  - (ii) gain of the first stage;
  - (iii) overall gain.
- (7 marks)
2. (a) State **three** merits of electronic oscillators. (3 marks)
- (b) With the aid of a labelled diagram, describe the operation of a colpitts oscillator. (8 marks)
- (c) A tank circuit of a colpitts oscillator has capacitors  $C_1$  and  $C_2$  of capacitance  $0.001\ \mu\text{F}$  and  $0.01\ \mu\text{F}$  respectively and inductance  $L$  of  $15\ \mu\text{H}$ . Determine the:
- (i) total capacitance;
  - (ii) operating frequency;
  - (iii) feedback fraction.
- (6 marks)
- (d) Draw a labelled block diagram of a three stage transistor amplifier. (3 marks)
3. (a) State **three** merits of using a silicon controlled rectifier (SCR) as a switch. (3 marks)
- (b) With the aid of a circuit diagram and output waveform, describe the SCR half-wave rectification. (6 marks)
- (c) An SCR half-wave rectifier circuit has a gate current of  $1\ \text{mA}$ . The forward breakdown voltage of the SCR is  $100\ \text{V}$ . If an a.c supply voltage of peak value  $200\ \text{V}$  is applied, determine the:
- (i) firing angle;
  - (ii) conducting angle;
  - (iii) average output voltage.
- (7 marks)
- (d) Explain each of the following as applied in operating amplifiers:
- (i) input offset current;
  - (ii) output offset voltage.
- (4 marks)

**SECTION B: DIGITAL ELECTRONICS**  
*Answer any **THREE** questions from this section.*

4. (a) Perform each of the following:
- (i) convert  $46.0625_{10}$  to binary;
  - (ii) convert  $A6E.9B_{16}$  to octal;
  - (iii)  $(1111.0111)_2 + (101.1001)_2$ .
- (9 marks)
- (b) State the number of bits in each of the following:
- (i) nibble;
  - (ii) byte.
- (2 marks)
- (c) Using 8-bits two's complement method perform each of the following:
- (i)  $F_{16} - 1E_{16}$ ;
  - (ii)  $-14_{10} - 18_{10}$ .
- (9 marks)
5. (a) State **three** application areas of flip-flops. (3 marks)
- (b) (i) Draw the truth table for a T-flip-flop.  
(ii) Illustrate how a J-K flip-flop can be modified to a T-flip-flop. (7 marks)
- (c) (i) Using D-flip flops, draw a block schematic diagram of a 4-bit serial-in-serial out (SISO) shift register.  
(ii) Describe the operation of the shift register in c (i). (8 marks)
- (d) Draw a labelled block diagram of a 2-to-4 decoder. (2 marks)
6. (a) Table 1 shows Boolean expressions for OR gate function. Complete the table. (4 marks)

**Table 1**

Boolean expression	Output
$A + 0$	
$A + 1$	
$A + \bar{A}$	
$A + A$	

(b) Simplify each of the following Boolean expressions:

(i)  $(\bar{X} + Y) \cdot (\bar{X} + Z)$ ;

(ii)  $A \bar{B} \bar{C} + \bar{A} \bar{B} C + A \bar{B} C + \bar{A} B \bar{C}$ .

(8 marks)

(c) (i) Define fan-in with respect to logic gates.

(ii) **Figure 3** shows a circuit diagram of a digital logic gate.

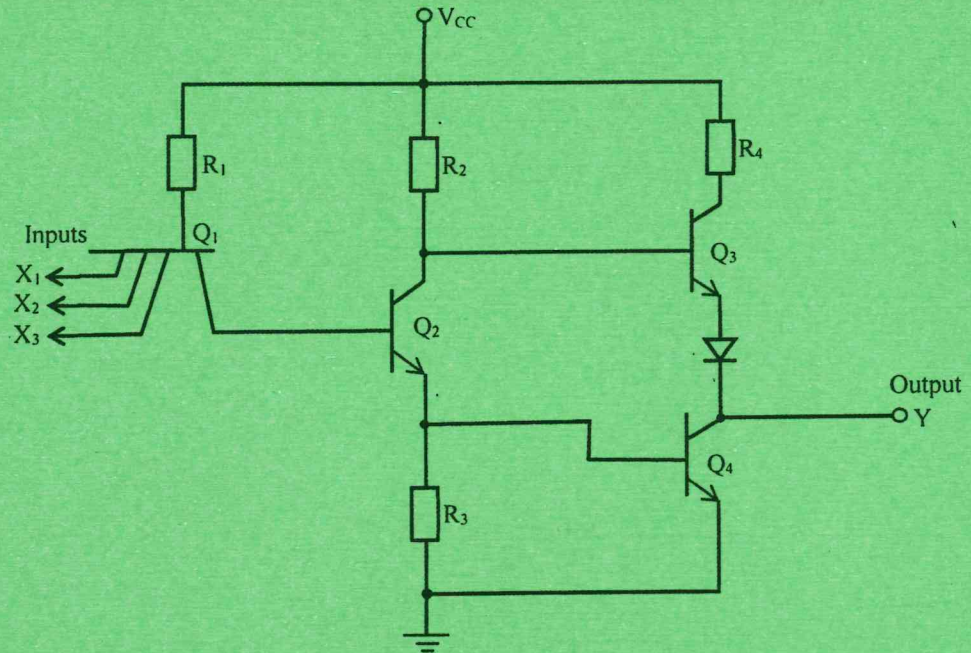


Fig. 3

- (I) identify the logic gate family;
- (II) with the aid of the truth table, explain the working of the gate;
- (III) state the logic gate type.

(8 marks)

7. (a) A combinational logic circuit has three inputs and one output. The output is equal to logic 1 under the following conditions:

- All inputs are equal to logic 1;
- None of the inputs are equal to logic 1;
- An ODD number of inputs are equal to logic 1.

- (i) obtain the truth table for the circuit;
- (ii) using a K-map, obtain a simplified expression for the sum-of-products (SOPs).
- (iii) draw the logic circuit using logic gates from the simplified expression in (ii).

(11 marks)

(b) A logic circuit is defined by the Boolean function  $Q = \overline{A}BC + A\overline{B}C$ . Implement the circuit using:

- (i) a decoder and gates only;
- (ii) half adder logic circuits only.

(9 marks)

8. (a) Define a synchronous counter, citing an example. (2 marks)

(b) Figure 4 shows a transition diagram of an asynchronous counter.

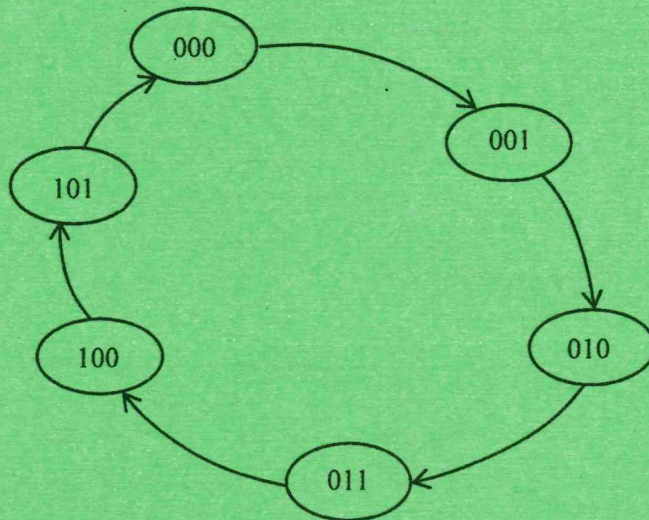


Fig. 4

- (i) determine its MODULO;
- (ii) draw the counter using D flip-flops.

(5 marks)

(c) (i) State two advantages of flash disks over magnetic tapes.

(ii) For a  $32K \times 16$  microcomputer ROM memory determine:

- (I) number of address lines;
- (II) word size;
- (III) capacity in kilobytes.

(7 marks)

(d) A  $64K \times 8$  memory is made up of four regions ROM, RAM, PROM and I/O devices following in that order. If each region has equal capacity and ROM starts at address  $0000H$  draw the system memory map. (6 marks)

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