2507/302
MICROCONTROLLER TECHNOLOGY
June/July 2020
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING (AVIONICS OPTION)
MODULE III

MICROCONTROLLER TECHNOLOGY

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:
Answer booklet;
Scientific calculator;
8051 Instruction set.

*Answer any **FIVE** of the **EIGHT** questions in the answer booklet provided.*
All questions carry equal marks.
Maximum marks for each part of a question are as shown.
Candidates should answer the questions in English.

This paper consists of 10 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

1. (a) Table 1 shows the features of the 8051 microcontroller. Complete the table.

(4 marks) ✓

Table 1

	Feature	Size
(i)	Data bus	
(ii)	Number of pins	
(iii)	Clock speed	
(iv)	Power supply	

(b) Convert:

(i) $ABEF_{16}$ into octal; ✓

(ii) 10110.01011_2 into Hexadecimal. 16.

(6 marks)

(c) Evaluate:

(i) $110011_2 - 101101_2$;

(ii) $100001_2 \div 110_2$;

(iii) $110011_2 \times 1101_2$.

(8 marks)

(d) State **two** advantages of circuits for two's complement operations over those for one's complement.

(2 marks)

2. (a) State **two** examples of:

(i) Proximity switches; ?

(ii) Displacement sensors.

(4 marks)

(b) Draw a labelled diagram of PLC architecture and state the function of each part.

(9 marks) ✓

(c) Figure 1 shows a microcontroller stack memory and register contents.

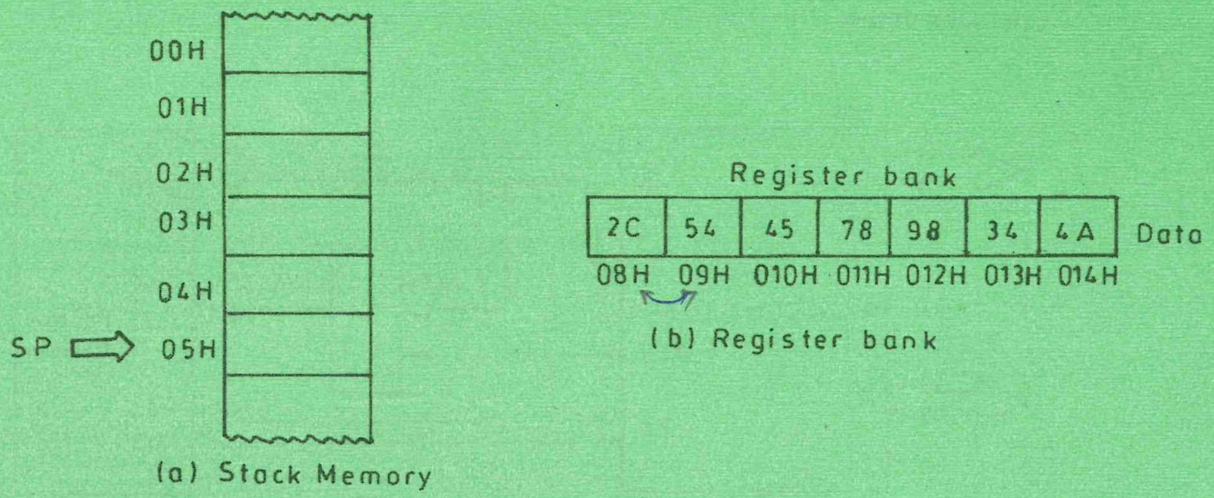

Fig. 1

(i) Write an assembly language program to exchange the contents of memory locations 08H and 09H using stack operations.

(ii) indicate the stack contents at the end of the program execution.

(iii) State the position of the stack points (SP) register at the end of program execution. (7 marks)

3. (a) With the aid of a flowchart, describe the fetch-execute sequence in a microcontroller. (7 marks)

(b) Draw ladder symbols for each of the following:

(i) Normally open contact (NO);

(ii) NOR gate. (3 marks)

(c) An aerospace plant uses four sensors A, B, C and D to control a conveyor belt at an assembly line. The conveyor will move when any of the following conditions are met:

- All sensors are low;
- Only one sensor output is high;
- Sensor A and D are low while B and C are high;
- Sensor A and D are high while B and C are low.

(i) Draw a truth table representations for the conditions

(ii) Write down the booleon logic expression for the conditions.

(iii) Implement the logic expression in C(ii) using PLC function block diagram. (10 marks)

4. (a) Figure 2 shows a schematic block diagram of a microcontroller interfaced to an external memory.

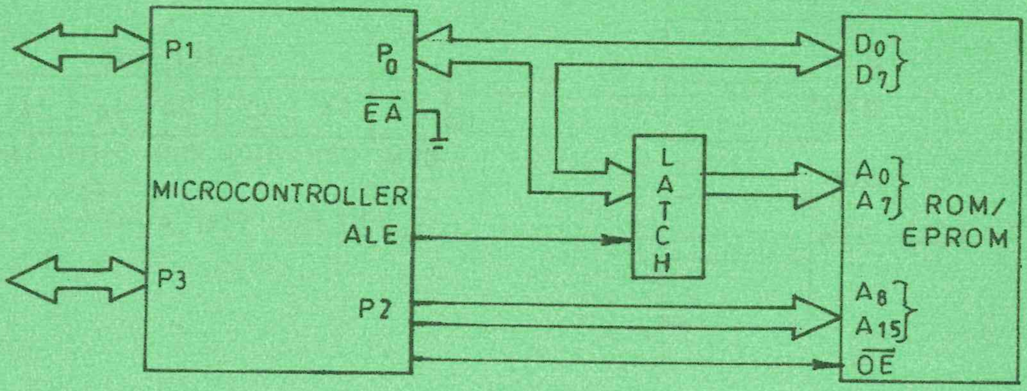

Fig.2

Explain

(i) function of the latch;

(ii) process of fetching data from the external memory location FFEOH.

(8 marks)

(b) Table 2 represents an 8051 microcontroller program.

Table 2

LINE	CODE		
1	MONITOR EQU 0000H		
2	ORG 8000 H		
3	MOV DPTR, #9000H		
4	MOVX A,@DPTR	E0	
5	MOV R1,A	F9	- Registers direct
6	INC DPTR		
7	MOVXA,@DPTR	E0	
8	INCR DPTR		
9	ADD A,R1	29	
10	DAA	D4	
11	MOVX@ DPTR, A	F0	
12	LJMP MONITOR	·	→ 02 | 0000 | ?
13	END		

(i) Identify **two** assembler directives in the program.

(ii) State the addressing mode used for the instruction in lines 3, 5 and 12.

(iii) Hand code the program into its equivalent machine code. (12 marks)

5. (a) Figure 3 represents PLC module wiring system used to control lamp X from either two different positions, S_0 and S_1.

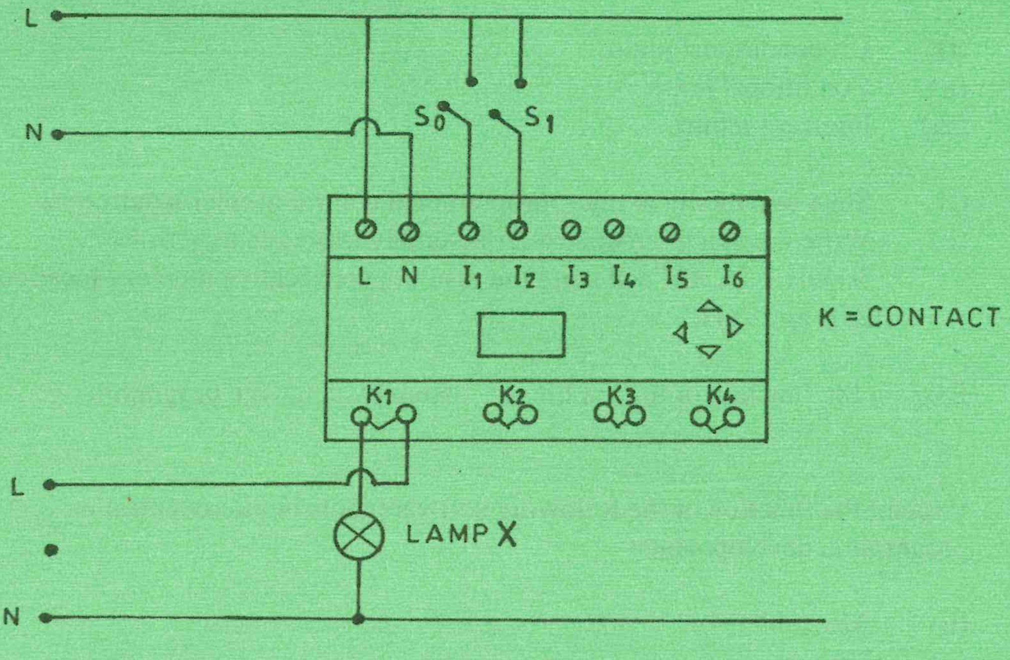

Fig. 3

?? (i) Draw the line circuit diagram of the system.

(ii) Write down a program listing for controlling the lamp. (7 marks)

(b) (i) State **two** application areas of SCADA systems.

(ii) With the aid of block diagram, describe the following SCADA architectures:

(I) Monolithic;

(iii) Distributed. (10 marks)

WAN

RTU

(c) State **three** distinct types of memories used with mircocontrollers. (3 marks)

CRTU

Legacy RTU

6. (a) Explain each of the following:

(i) Watchdog timer in microcontrollers;
(ii) Data loggers in SCADA system. (6 marks)

(b) With the aid of a one line instruction, describe each of the following control transfer operations in microcontrollers:

(i) Un-conditional jump;
(ii) Conditional jump;
(iii) Interrupt return. (6 marks)

(c) (i) State two merits of microprogrammed control in microcontrollers.
(ii) Write down a microcontroller assembly language to perform: 3040H + 2C30H and store the result in consecutive memory locations 25H and 26H. (8 marks)

7. (a) Explain the function of the list file in a assembly language programming.
– Specify instructions – drive bits used in program
– Sequence of instructions
(3 marks)

(b) Explain the function of the following software tools in microcontroller programme development:

(ii) Assembler;
(ii) Linker;
(iii) Debbuger;
(iv) Monitor. (8 marks)

(c) (i) Describe each of the following interrupt registers in microcontroller:
enables Interrupt Service Routine (ISR) to function depending if or not higher priority bit is working

(I) Interrupt Enable (IE) register;
(II) Interrupt priority (IP) register; schedules interrupt based on priority High priority – Low interrupt velocity (vice versa) true
(III) Timer control (T CON) register. Sequences delay time PWM
Gen delay

(ii) State **three** types of interrupt in a microcontroller. (9 marks)

8. (a) State **two** differences between RAM and ROM in a microcontroller. (4 marks)

(b) Figure 4 represents a DAC 0808 intefaced to an 8051 microcontroller.

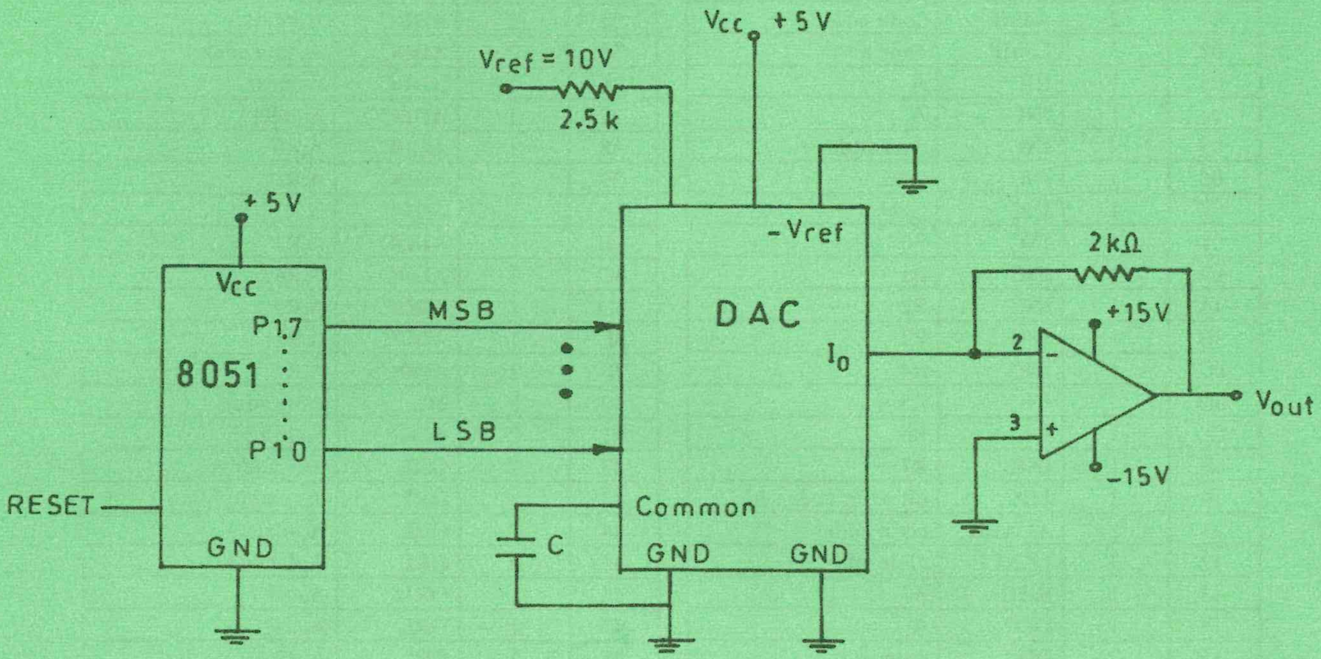

Fig. 4

(i) Given that the input data from the microcontroller is F1 H.
Determine the:
(I) Output current;
(II) Output voltage.

(ii) Write an assembly language program for the microcontroller to generate a triangular waveform. (12 marks)

(c) State:

(i) **two** uses of memories in microcontrollers.
(ii) **two** merits of semiconductors memories in digital circuits.

(4 marks)

Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	code addr
02	3	LJMP	code addr
03	1	RR	A
04	1	INC	A
05	2	INC	data addr
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	bit addr, code addr
11	2	ACALL	code addr
12	3	LCALL	code addr
13	1	RRC	A
14	1	DEC	A
15	2	DEC	data addr
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	bit addr, code addr
21	2	AJMP	code addr
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,data addr
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	bit addr, code addr
31	2	ACALL	code addr
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#data
35	2	ADDC	A,data addr
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R6
3F	1	ADDC	A,R7
40	2	JC	code addr
41	2	AJMP	code addr
42	2	ORL	data addr,A
43	3	ORL	data addr,#data
44	2	ORL	A,#data
45	2	ORL	A,data addr
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	code addr
51	2	ACALL	code addr
52	2	ANL	data addr,A
53	3	ANL	data addr,#data
54	2	ANL	A,#data
55	2	ANL	A,data addr
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	code addr
61	2	AJMP	code addr

8051 OpCodes en Hexadecinal.

62	2	XRL	data addr,A
63	3	XRL	data addr,#data
64	2	XRL	A,#data
65	2	XRL	A,data addr
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	code addr
71	2	ACALL	code addr
72	2	ORL	C,bit addr
73	1	JMP	@A+DPTR
74	2	MOV	A,#data
75	3	MOV	data addr,#data
76	2	MOV	@R0,#data
77	2	MOV	@R1,#data
78	2	MOV	R0,#data
79	2	MOV	R1,#data
7A	2	MOV	R2,#data
7B	2	MOV	R3,#data
7C	2	MOV	R4,#data
7D	2	MOV	R5,#data
7E	2	MOV	R6,#data
7F	2	MOV	R7,#data
80	2	SJMP	code addr
81	2	AJMP	code addr
82	2	ANL	C,bit addr
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	data addr, data addr
86	2	MOV	data addr,@R0
87	2	MOV	data addr,@R1
88	2	MOV	data addr,R0
89	2	MOV	data addr,R1
8A	2	MOV	data addr,R2
8B	2	MOV	data addr,R3
8C	2	MOV	data addr,R4
8D	2	MOV	data addr,R5
8E	2	MOV	data addr,R6
8F	2	MOV	data addr,R7
90	3	MOV	DPTR,#data
91	2	ACALL	code addr
92	2	MOV	bit addr,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#data
95	2	SUBB	A,data addr
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/bit addr
A1	2	AJMP	code addr
A2	2	MOV	C,bit addr
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,data addr
A7	2	MOV	@R1,data addr
A8	2	MOV	R0,data addr
A9	2	MOV	R1,data addr
AA	2	MOV	R2,data addr
AB	2	MOV	R3,data addr
AC	2	MOV	R4,data addr
AD	2	MOV	R5,data addr
AE	2	MOV	R6,data addr
AF	2	MOV	R7,data addr
B0	2	ANL	C,/bit addr
B1	2	ACALL	code addr
B2	2	CPL	bit addr
B3	1	CPL	C
B4	3	CJNE	A,#data,code addr
B5	3	CJNE	A,data addr,code addr
B6	3	CJNE	@R0,#data,code addr
B7	3	CJNE	@R1,#data,code addr
B8	3	CJNE	R0,#data,code addr
B9	3	CJNE	R1,#data,code addr
BA	3	CJNE	R2,#data,code addr
BB	3	CJNE	R3,#data,code addr
BC	3	CJNE	R4,#data,code addr
BD	3	CJNE	R5,#data,code addr
BE	3	CJNE	R6,#data,code addr
BF	3	CJNE	R7,#data,code addr
C0	2	PUSH	data addr
C1	2	AJMP	code addr
C2	2	CLR	bit addr
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,data addr
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1

8051 OpCodes en Hexadecinal.

C8	1	**XCH**	A,R0
C9	1	**XCH**	A,R1
CA	1	**XCH**	A,R2
CB	1	**XCH**	A,R3
CC	1	**XCH**	A,R4
CD	1	**XCH**	A,R5
CE	1	**XCH**	A,R6
CF	1	**XCH**	A,R7
D0	2	**POP**	data addr
D1	2	**ACALL**	code addr
D2	2	**SETB**	bit addr
D3	1	**SETB**	C
D4	1	**DA**	A
D5	3	**DJNZ**	data addr,code addr
D6	1	**XCHD**	A,@R0
D7	1	**XCHD**	A,@R1
D8	2	**DJNZ**	R0,code addr
D9	2	**DJNZ**	R1,code addr
DA	2	**DJNZ**	R2,code addr
DB	2	**DJNZ**	R3,code addr
DC	2	**DJNZ**	R4,code addr
DD	2	**DJNZ**	R5,code addr
DE	2	**DJNZ**	R6,code addr
DF	2	**DJNZ**	R7,code addr
E0	1	**MOVX**	A,@DPTR
E1	2	**AJMP**	code addr
E2	1	**MOVX**	A,@R0
E3	1	**MOVX**	A,@R1
E4	1	**CLR**	A
E5	2	**MOV**	A,data addr
E6	1	**MOV**	A,@R0
E7	1	**MOV**	A,@R1
E8	1	**MOV**	A,R0
E9	1	**MOV**	A,R1
EA	1	**MOV**	A,R2
EB	1	**MOV**	A,R3
EC	1	**MOV**	A,R4
ED	1	**MOV**	A,R5
EE	1	**MOV**	A,R6
EF	1	**MOV**	A,R7
F0	1	**MOVX**	@DPTR,A
F1	2	**ACALL**	code addr
F2	1	**MOVX**	@R0,A
F3	1	**MOVX**	@R1,A
F4	1	**CPL**	A
F5	2	**MOV**	data addr,A
F6	1	**MOV**	@R0,A
F7	1	**MOV**	@R1,A
F8	1	**MOV**	R0,A
F9	1	**MOV**	R1,A
FA	1	**MOV**	R2,A
FB	1	**MOV**	R3,A
FC	1	**MOV**	R4,A
FD	1	**MOV**	R5,A
FE	1	**MOV**	R6,A
FF	1	**MOV**	R7,A

Instruction Opcodes in Hexadecimal Order

8051 OpCodes en Hexadecinal.

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