2506/202
2507/202
ELECTRONICS AND CONTROL SYSTEMS
Oct. /Nov. 2019
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING
(AIRFRAMES AND ENGINES OPTION)
(AVIONICS OPTION)

MODULE II

ELECTRONICS AND CONTROL SYSTEMS

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:
answer booklet;
non-programmable scientific calculator;
Log-linear graph paper.
*This paper consists of **EIGHT** questions in **TWO** sections; **A** and **B**.*
*Answer **THREE** questions from section **A** and **TWO** questions from section **B** in the answer booklet provided.*
All questions carry equal marks.
Maximum marks for each part of a question are as indicated.
Candidates should answer the questions in English.

This paper consists of 7 printed pages and 1 insert.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

Turn over

SECTION A: ELECTRONICS

*Answer **THREE** questions from this section.*

1. (a) Differentiate between intrinsic and extrinsic semiconductors. (2 marks)

(b) With the aid of a V-I characteristic curve explain the operation of a zener-diode. (7 marks)

(c) Figure 1 shows a common-emitter silicon transistor amplifier circuit diagram using a fixed-bias.

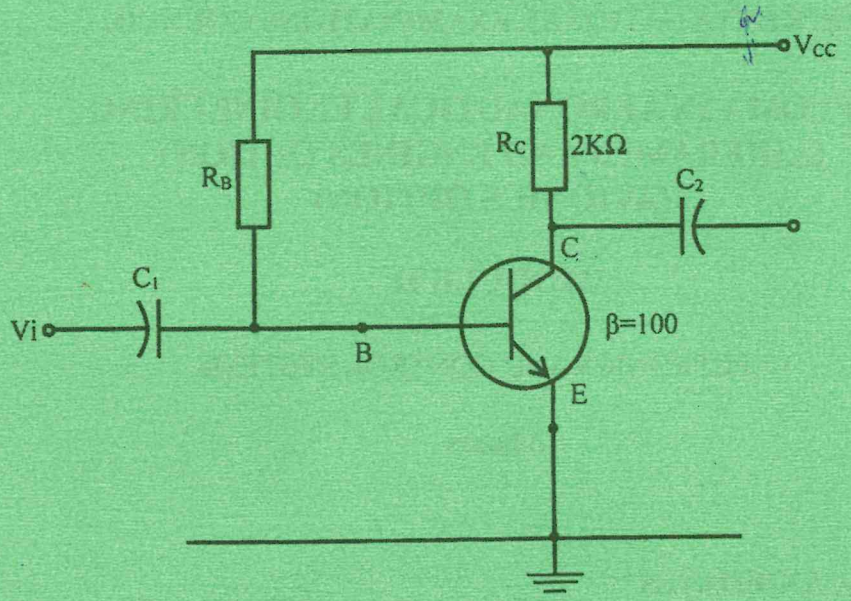

Fig. 1

The transistor is operated at $I_C = 1$ mA, $V_{CE} = 4$V.
Determine the:

(i) supply voltage, V_{CC};
(ii) value of base resistor, R_B.

(7 marks)

(d) A two-stage common-emitter RC - coupled amplifier uses two similar, transistors whose h-parameter and internal capacitances are $h_{fe} = 600$, hie = 10 kΩ, $C_{bc} = 2.5$ pF and $C_{be} = 9$ PF. The coupling capacitor is 0.5 μF and the load resistance is 10 kΩ.
Determine the:

(i) mid-frequency gain of the first stage;
(ii) lower cut-off frequency.

(4 marks)

2. (a) (i) With the aid of a circuit diagram, describe the operation of a half-bridge controlled inverter.

(ii) State **two** areas of application of inverters.

(8 marks)

(b) Figure 2 shows a circuit diagram of a Colpitt's oscillator.

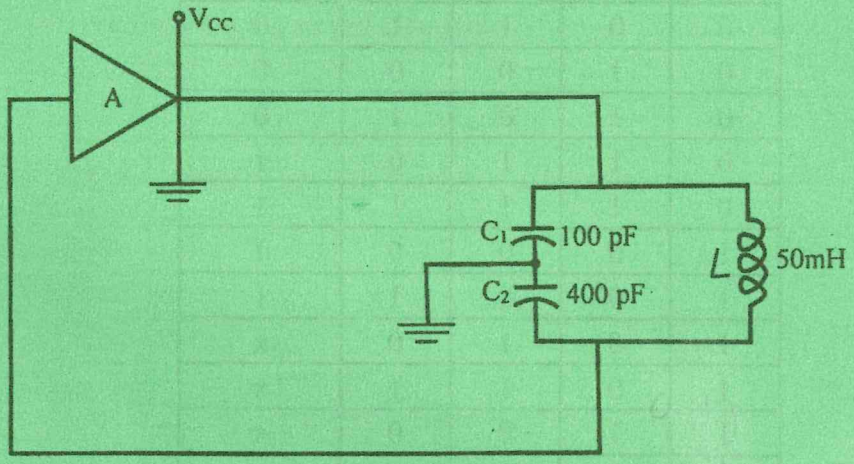

Fig. 2

Determine the:

(i) frequency of oscillation;
(ii) feedback factor;
(iii) minimum gain.

(8 marks)

(c) (i) Distinguish between monostable and bistable multivibrators.

(ii) State **two** merits of using LEDs as displays.

Long life.
Low power consumption

(4 marks)

3. (a) Convert the decimal number 43 into:

(i) octal;
(ii) excess - 3 code;
(iii) binary.

(6 marks)

(b) Prove the following identity using Boolean algebra:

$A \oplus B \oplus AB = A + B$

(6 marks)

Table 1

Inputs				Output
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	x
1	0	1	1	x
1	1	0	0	x
1	1	0	1	x
1	1	1	0	x
1	1	1	1	x

(i) Using a K-map, derive the minimum logic expression for Y.

(ii) Implement Y using NAND gates only.

(8 marks)

4. (a) Define each of the following with respect to logic gates:

(i) fan-out;
(ii) power dissipation.

(2 marks)

(b) State **two** merits of Emitter-Coupled logic (ECL) gates. (2 marks)

(c) An asynchronous counter counts from 0 to 12.

(i) Determine the number of flip-flops required to implement it;

(ii) Draw the logic circuit diagram of the counter, using JK flip-flop.

(7 marks)

(d) (i) Draw a circuit diagram of a CMOS NAND gate and describe its operation.

(ii) State **three** advantages of CMOS gates over TTL gates.

(9 marks)

5. (a) (i) Draw a truth table of a binary full-adder.

(ii) Realise the full adder circuit using:

(I) 3 to 8 decoder and OR-gates;
(II) 4 x 1 multiplexers.

(10 marks)

(b) Define each of the following with respect to computer memories:

(i) cache;
(ii) access time.

(2 marks)

(c) (i) A microcomputer requires 32k X 8 RAM memory. This is implemented using 8k X 8 RAM chips. Determine the:

(I) number of chips required;
(II) number of address lines for each 8k X 8 chips.

(ii) Draw a schematic block diagram for the implementation of the memory in c(i).

(8 marks)

SECTION B: CONTROL SYSTEMS

*Answer **TWO** questions from this section.*

6. (a) Define each for the following with respect to control systems:

(i) control action;
(ii) feedback;
(iii) disturbance.

(3 marks)

(b) Figure 3 shows a block diagram of a control system.

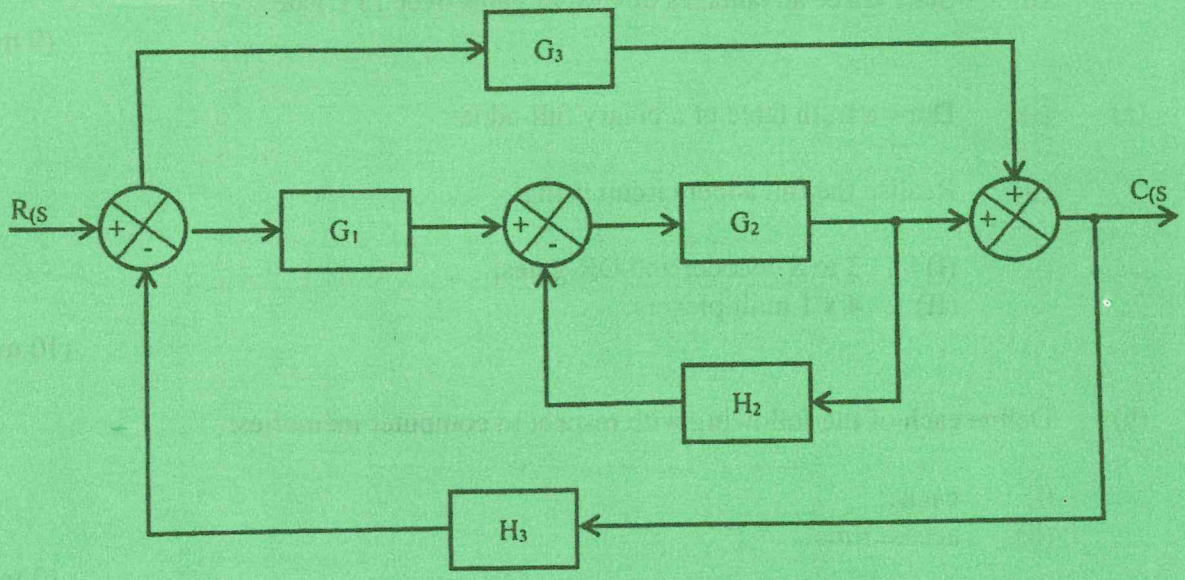

Fig. 3

(i) Draw a signal flow graph for the block diagram.

(ii) Use Mason's gain formula to determine the transfer function.

(14 marks)

(c) State **three** effects of a phase-lead compensation control network on a system.

(3 marks)

7. (a) State **three** reasons why Bode plots are preferred in system analysis to Nyquist plots.

(3 marks)

(b) Outline the procedure for obtaining the Bode plot of a given transfer function.

(5 marks)

(c) (i) Using asymptotic approximations, plot the Bode diagram for the following transfer function:

$$G(S) = \frac{10}{S(1+0.4S)(1+0.1S)}$$

(ii) From the Bode plot in c(i), obtain the:

(I) gain margin;
(II) phase margin.

(12 marks)

8. (a) State the Routh-Hurwitz stability criterion. (2 marks)

(b) The open-loop transfer function of a unity feedback system is given by:

$$G(s) = \frac{0.382k}{S(1+0.1S)(1+0.06S)}$$

Using the Routh array, determine the limiting value of K for the system to be stable.
(6 marks)

(c) (i) Draw analogue computing symbols for each of the following:

(I) integrator;
(II) summer.

(ii) State **two** merits of analogue computer simulation in control system design.
(4 marks)

(d) A unity feedback control system has an open loop transfer function given by:

$$G(s) = \frac{1}{S(S+1)(S+2)}$$

Draw an analogue computer simulation diagram for the closed-loop system.
(8 marks)

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