2207/304
DIGITAL PRINCIPLES AND MICROPROCESSORS
Oct./Nov. 2019
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING AVIONICS (COMMUNICATION AND NAVIGATION OPTION)

DIGITAL PRINCIPLES AND MICROPROCESSORS

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:
- *Answer booklet;*
- *Non programmable scientific calculator;*
- *8080/8085 Instruction set;*
- *Drawing instruments.*

*Answer **FIVE** of the **EIGHT** questions in the answer booklet provided.*
All questions carry equal marks.
Maximum marks for each part of a question are as shown.
Candidates should answer the questions in English.

This paper consists of 7 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

1. (a) Convert the decimal number 22.34375_{10} into:

(i) binary;
(ii) octal;
(iii) hexadecimal.

(7 marks)

(b) Evaluate each of the following in the given bases:

(i) $(FD\ 16)_{16}$
$(CE\ 2F)_{16}$

(ii) $(1001_2 - 1110_2)$ using 8-bits, two's complement.

(iii) $111_2 \times 101_2$. (7 marks)

(c) (i) Convert the decimal number 367_{10} into:

(I) 8-4-2-1 BCD code;
(II) EXcess-3 code.

(ii) Convert the binary number 101110_2 into gray code. (6 marks)

2. (a) For a two input XOR gate, draw its:

(i) truth table;
(ii) logic symbol.

(4 marks)

(b) (i) State the following Boolean laws for three variables, A, B and C:

(I) associative;
(II) distributive.

(ii) Simplify the following Boolean expression using De'Morgan's theorem:

$$Q = \overline{X\overline{Y}(X+Z)}.$$

(7 marks)

(c) A logic circuit is required to monitor three elevators A, B and C. Anytime at least two of the three elevators are at ground level, a logic 1 at the output of the circuit triggers an alarm, Q. By taking logic 1 to represent elevator at ground level.

(i) draw a truth table representation of the system;
(ii) with the aid of a K-map, obtain a simplified Boolean expression for the elevators control;
(iii) implement the expression in c (ii) using NAND gates only.

(9 marks)

3. (a) Define each of the following as used in flip-flops:

(i) set up time;
(ii) level triggered;
(iii) propagation delay.

(3 marks)

(b) With the aid of a logic diagram and truth table, explain the following as used in RS flip-flops:

(i) no change;
(ii) set;
(iii) invalid conditions.

(8 marks)

(c) With the aid of a logic diagram and truth table, explain the implementation of JK flip-flop using RS flip-flop and NAND gates. (9 marks)

4. (a) (i) State **two** applications of shift registers.
(ii) Figure 1 shows a 4-bit register.

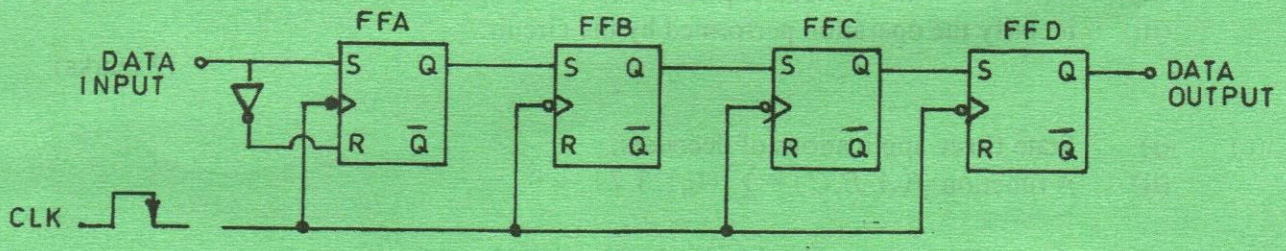

Fig.1

The flip-flops are reset at the beginning and the binary data value 1011_2 is fed into the input. Draw the timing waveforms to show the states of the flip-flops after 1, 2, 3 and 4 clock pulses. (7 marks)

(b) (i) Explain **one** advantage of synchronous counters over asynchronous counters.

(ii) Draw a schematic diagram representation of a MOD-6 asynchronous counter with active - high clock pulses using J - K flip-flops. (6 marks)

(c) A binary counter is needed to divide a 128 kHz square signal to a 4 kHz square signal. Determine the:

(i) modulus number of the counter;
(ii) frequency at the second flip-flop;
(iii) count after 132 pulses.

(7 marks)

5. (a) State:

(i) **two** types of parity in a data word;
(ii) **one** logic gate used to generate parity bits.

(3 marks)

(b) Figure 2 represents a logic circuit diagram.

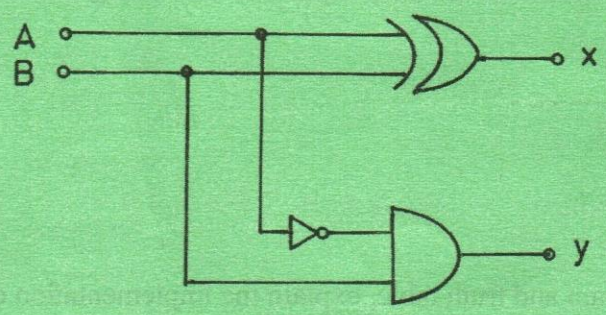

Fig. 2

(i) draw its truth table;
(ii) write down the Boolean expression for the outputs X and Y;
(iii) identify the operation performed by the circuit.

(7 marks)

(c) (i) State **three** applications of decoders;
(ii) A function $f(A,B,C)=\sum(0,1,3,7)$.

(I) Draw the truth table for the function.
(II) Implement the function using a decoder and a gate.

(10 marks)

6. (a) (i) State **three** application areas of Digital Analogue Converters (DAC).

(ii) Draw a circuit diagram of an OP-Amp based 4-bit weighted-resistor network DAC.

(iii) Write down the expression for the output voltage for the DAC in (a) (ii).

(7 marks)

(b) A 4-bits digital to analogue converter (DAC) has an output voltage of 8 V when the digital input is 1000_2. Determine the:

(i) output voltage when the digital input is 1011_2;
(ii) percentage resolution.

(4 marks)

(c) Table 1 shows an hexadecimal machine language program for 8085 microprocessor:

Table 1

Memory Address	OP CODE Hex
2000	21
2001	30
2002	F2
2003	11
2004	D0
2005	23
2006	46
2007	1A
2008	77
2009	78
200A	12
200B	76

(i) di-assemble the program into 8085 mnemonics.
(ii) state what the program accomplishes.

(9 marks)

7. (a) State the function of each of the following microprocessor registers and indicate their typical sizes in bits:

(i) accumulator;
(ii) instruction register;
(iii) stack pointer.

(6 marks)

(b) With the aid of a flow chart, write an assembly language program to sum five bytes stored in consecutive memory locations starting from 5001 H and store the results in memory location 500 A H.

(9 marks)

(c) A memory is organized as $4K \times 16$. Determine the:

(i) number of memory locations;
(ii) number of bits in each word;
(iii) total number of bits in the memory.

(5 marks)

8. (a) State:

(i) **three** functions of an input-output (I/O) interface;
(ii) **two** sources of interrupts in a computer.

(5 marks)

(b) Describe the following input-output techniques:

(i) programmed;
(ii) interrupt driven.

(4 marks)

(c) Draw a flow chart for a logical fault tracing method in a microprocessor based system.

(7 marks)

(d) State the symptom(s) for each of the following faults in a microcomputer:

(i) reset pin is permanently grounded;
(ii) IO/$\overline{M}$ stuck to logic 0.

(4 marks)

Instruction set of

8080/8085

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	2B	DCX H	56	MOV D,M	81	ADD C	AC	XRA H	D7	RST 2
01	LX1 B,D16	2C	INR L	57	MOV D,A	82	ADD D	AD	XRA L	D8	RC
02	STAX B	2D	DCR L	58	MOV E,B	83	ADD E	AE	XRA M	D9	–
03	INX B	2E	MVI L,D8	59	MOV E,C	84	ADD H	AF	XRA A	DA	JC Adr
04	INR B	2F	CMA	5A	MOV E,D	85	ADD L	B0	ORA B	DB	IN D8
05	DCR B	30	SIM	5B	MOV E,E	86	ADD M	B1	ORA C	DC	CC Adr
06	MVI B,D8	31	LXI SPD16	5C	MOV E,H	87	ADD A	B2	ORA D	DD	–
07	RLC	32	STA Adr	5D	MOV E,L	88	ADC B	B3	ORA E	DE	SBI D8
08	–	33	INX SP	5E	MOV E,M	89	ADC C	B4	ORA H	DF	RST 3
09	DAD B	34	INR M	5F	MOV E,A	8A	ADC D	B5	ORA L	E0	RPO
0A	LDAX B	35	DCR M	60	MOV H,B	8B	ADC E	B6	ORA M	E1	POP H
0B	DCX B	36	MVI M,D8	61	MOV H,C	8C	ADC H	B7	ORA A	E2	JPO Adr
0C	INR C	37	STC	62	MOV H,D	8D	ADC L	B8	CMP B	E3	XTHL
0D	DCR C	38	–	63	MOV H,E	8E	ADC M	B9	CMP C	E4	CPO Adr
0E	MVI C,D8	39	DAD SP	64	MOV H,H	8F	ADC A	BA	CMP D	E5	PUSH H
0F	RRC	3A	LDA Adr	65	MOV H,L	90	SUB B	BB	CMP E	E6	ANI D8
10	–	3B	DCX SP	66	MOV H,M	91	SUB C	BC	CMP H	E7	RST 4
11	LXI D,D16	3C	INR A	67	MOV H,A	92	SUB D	BD	CMP L	E8	RPE
12	STAX D	3D	DCR A	68	MOV L,B	93	SUB E	BE	CMP M	E9	PCHL
13	INX D	3E	MVI A,D8	69	MOV L,C	94	SUB H	BF	CMP A	EA	JPE Adr
14	INR D	3F	CMC	6A	MOV L,D	95	SUB L	C0	RNZ	EB	XCHG
15	DCR D	40	MOV B,B	6B	MOV L,E	96	SUB M	C1	POP B	EC	CPE Adr
16	MVI D,D8	41	MOV B,C	6C	MOV L,H	97	SUB A	C2	JNZ Adr	ED	–
17	RAL	42	MOV B,D	6D	MOV L,L	98	SBB B	C3	JMP Adr	EE	ERI D8
18	–	43	MOV B,E	6E	MOV L,M	99	SBB C	C4	CNZ Adr	EF	RST 5
19	DAD D	44	MOV B,H	6F	MOV L,A	9A	SBB D	C5	PUSH B	F0	RP
1A	LDAX D	45	MOV B,L	70	MOV M,B	9B	SBB E	C6	ADI D8	F1	POP PSW
1B	DCX D	46	MOV B,M	71	MOV M,C	9C	SBB H	C7	RST 0	F2	JP Adr
1C	INR E	47	MOV B,A	72	MOV M,D	9D	SBB L	C8	RZ	F3	DI
1D	DRC E	48	MOV C,B	73	MOV M,E	9E	SBB M	C9	RET Adr	F4	CP Adr
1E	MVI E,D8	49	MOV C,C	74	MOV M,H	9F	SBB A	CA	JZ	F5	PUSH PSW
1F	RAR	4A	MOV C,D	75	MOV M,L	A0	ANA B	CB	–	F6	ORI D8
20	RIM	4B	MOV C,E	76	HLT	A1	ANA C	CC	CZ Adr	F7	RST 6
21	LXI H,D16	4C	MOV C,H	77	MOV M,A	A2	ANA D	CD	CALL Adr	F8	RM
22	SHLD Adr	4D	MOV C,L	78	MOV A,B	A3	ANA E	CE	ACI D8	F9	SPHL
23	INX H	4E	MOV C,M	79	MOV A,C	A4	ANA H	CF	RST 1	FA	JM Adr
24	INR H	4F	MOV C,A	7A	MOV A,D	A5	ANA L	D0	RNC	FB	EI
25	DCR H	50	MOV D,B	7B	MOV A,E	A6	ANA M	D1	POP D	FC	CM Adr
26	MVI H,D8	51	MOV D,C	7C	MOV A,H	A7	ANA A	D2	JNC Adr	FD	–
27	DAA	52	MOV D,D	7D	MOV A,L	A8	XRA B	D3	OUT D8	FE	CPI D8
28	–	53	MOV D,E	7E	MOV A,M	A9	XRA C	D4	CNC Adr	FF	RST 7
29	DAD H	54	MOV D,H	7F	MOV A,A	AA	XRA D	D5	PUSH D		
2A	LHLD Adr	55	MOV D,L	80	ADD B	AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity. D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. Adr = 16-bit address.

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