2207/304
DIGITAL PRINCIPLES
AND MICROPROCESSORS
June/July 2019
Time: 3 hours

THE KENYA NATIONAL EXAMINATIONS COUNCIL

DIPLOMA IN AERONAUTICAL ENGINEERING (AVIONICS) (COMMUNICATION AND NAVIGATION OPTION)

DIGITAL PRINCIPLES AND MICROPROCESSORS

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:
Answer booklet;
8080/8085 micro processer instructions;
Non-programmable scientific calculator.
*Answer any **FIVE** of the **EIGHT** questions in the answer booklet provided.*
All questions carry equal marks.
Maximum marks for each part of a question are as shown.
Candidates should answer the questions in English.

This paper consists of 6 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

Turn over

1. (a) (i) Outline the steps involved in gray code to binary conversions.

(ii) Perform each of the following conversions:

I. 403_{10} into excess - 3 code;

II. $9B2.1A_{16}$ into decimal. (9 marks)

(b) Evaluate each of the following:

(i) $110.10_2 \times 10.1_2$;

(ii) $11110110_2 \div 110_2$;

(iii) $1A8_{16} + AF_{16}$. (9 marks)

(c) Draw a truth table for a 2-bit binary to gray code converter. (2 marks)

2. (a) Perform each of the following using Boolean algebra:

(i) $A(\overline{A}+1)$;

(ii) $B(B+\overline{B})$. (4 marks)

(b) (i) Simply the expression $F = \overline{ABC} + \overline{C}.\overline{D}$ using Demorgan's theorem.

(ii) Convert the expression $Y = AC + AB + BC$ into canonical SOP form. (7 marks)

(c) (i) Simplify the Boolean function:

$f(x,y,z) = \sum(2,3,4,5)$ using a Khanauph map.

(ii) Draw the logic diagram for the logic expression. (9 marks)

3. (a) Define each of the following with respect to flip-flops:

(i) propagation delay;

(ii) hold time;

(iii) set-up time. (3 marks)

(b) Draw the symbol of a D-type flip-flop and its truth table. (6 marks)

(c) (i) State the merit of synchronous counters.

(ii) I. Draw a table for the counting sequence of an asynchronous decade counter.

II. Implement the counter in (b)(ii) I using JK flip-flops. (9 marks)

(d) State **two** applications of counters. (2 marks)

(a) A burglar alarm system has three sensors (A, B and C). The alarm should sound if two or more sensors are activated, i.e logic 1.

(i) Draw the truth table;
(ii) Write the logic expression for the alarm;
(iii) Simplify the expression in (b)(ii);
(iv) Implement the simplified expression using logic gates. (10 marks)

(b) (i) Figure 1 shows a schematic block diagram of a successive approximation analog-to-digital converter (ADC). Describe its operation.

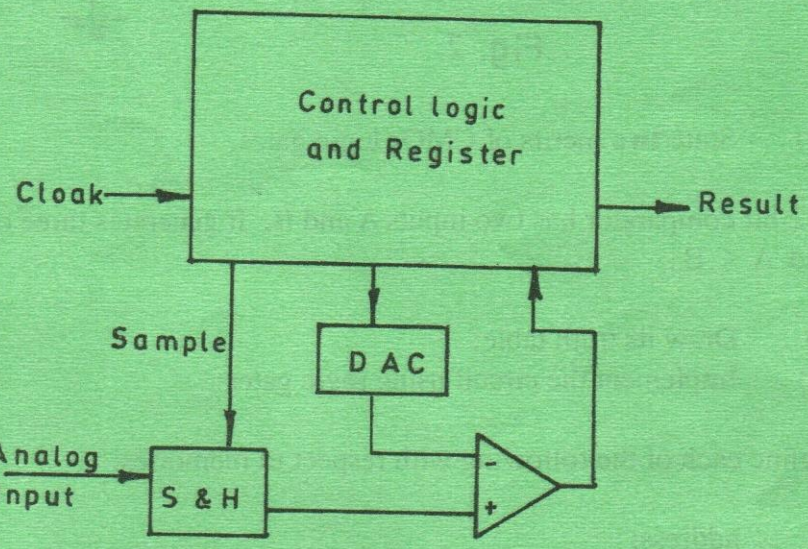

Fig. 1

(ii) An analogue to Digital Converter has a resolution of 5 mV and full scale voltage is 15 V. Determine the number of bits. (10 marks)

5. (a) Define each of the following with respect to logic families:

(i) power dissipation;
(ii) noise margin;
(iii) fan in. (3 marks)

(b) (i) Figure 2 shows a circuit diagram of a CMOs gate. Describe its operation hence deduce the logic function it performs.

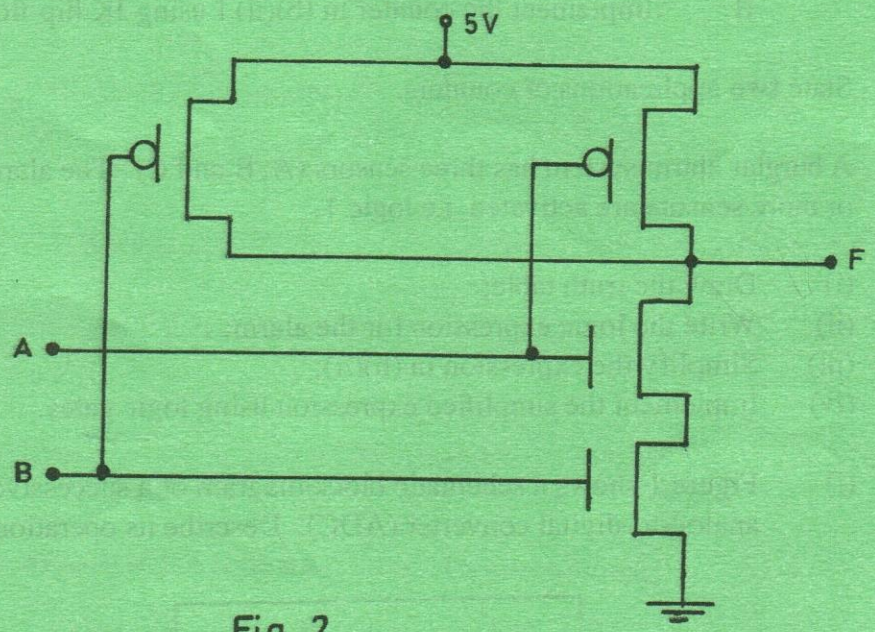

Fig. 2

(ii) State **two** merits of CMOs logic gates. (7 marks)

(c) A 2-bit comparator has two inputs A and B. It generates three outputs $A > B$, $A = B$ and $A < B$.

(i) Draw its truth table;
(ii) Implement the circuit using logic gates. (10 marks)

6. (a) Define each of the following with respect to memories:

(i) address;
(ii) capacity. (2 marks)

(b) State the functions of each of the following pins of a memory IC:

(i) address line;
(ii) chip enable. (2 marks)

(c) A 1 kilobyte RAM is to be implemented using 512 byte x 8 memory chips.

(i) Determine the:

I. number of chips required;
II. number of address lines for each memory chip.

(ii) Draw the memory implementation diagram. (8 marks)

(d) With the aid of a diagram, explain the use of a logic analyser in microprocessor fault diagnosis. (8 marks)

7. (a) State the functions of each of the following components of a microprocessor:

(i) instruction register;
(ii) arithmetic logic unit;
(iii) buffer register.
(3 marks)

(b) Distinguish between hard wired and micro programmed control units. (2 marks)

(c) With the aid of a flowchart, describe the microprocessor instruction fetch-execute cycle. (8 marks)

(d) Write an assembly language program that multiplies by 10 the content of memory location 8000 H and transfers the result to memory location 6200 H. (7 marks)

8. (a) Explain the functions of each of the following in assembly language programming:

(i) loader;
(ii) debugger.
(4 marks)

(b) Differentiate between a one pass assembler and a two pass assembler. (2 marks)

(c) Table 1 shows an assembly language program segment. Translate it into its equivalent hexadecimal machine code. (7 marks)

Table 1

ORG C000 H
XRA A
LHLD LIST
MOV A, L
NOP
ADD H
STA MEM
HLT
ORG D000 H
LIST: DB 2, 4;
MEM: ORG D00A H

(d) (i) State **three** functions of I/0 interfaces.

(ii) Explain the operation of a direct memory access (DMA) controller. (7 marks)

Instruction set of

8080/8085

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	28	DCX H	56	MOV D,M	81	ADD C	AC	XRA H	D7	RST 2
01	LX1 B,D16	2C	INR L	57	MOV D,A	82	ADD D	AD	XRA L	D8	RC
02	STAX B	2D	DCR L	58	MOV E,B	83	ADD E	AE	XRA M	D9	–
03	INX B	2E	MVI L,D8	59	MOV E,C	84	ADD H	AF	XRA A	DA	JC Adr
04	INR B	2F	CMA	5A	MOV E,D	85	ADD L	B0	ORA B	DB	IN D8
05	DCR B	30	SIM	5B	MOV E,E	86	ADD M	B1	ORA C	DC	CC Adr
06	MVI B,D8	31	LXI SPD16	5C	MOV E,H	87	ADD A	B2	ORA D	DD	–
07	RLC	32	STA Adr	5D	MOV E,L	88	ADC B	B3	ORA E	DE	SBI D8
08	–	33	INX SP	5E	MOV E,M	89	ADC C	B4	ORA H	DF	RST 3
09	DAD B	34	INR M	5F	MOV E,A	8A	ADC D	B5	ORA L	E0	RPO
0A	LDAX B	35	DCR M	60	MOV H,B	8B	ADC E	B6	ORA M	E1	POP H
0B	DCX B	36	MVI M,D8	61	MOV H,C	8C	ADC H	B7	ORA A	E2	JPO Adr
0C	INR C	37	STC	62	MOV H,D	8D	ADC L	B8	CMP B	E3	XTHL
0D	DCR C	38	– –	63	MOV H,E	8E	ADC M	B9	CMP C	E4	CPO Adr
0E	MVI C,D8	39	DAD SP	64	MOV H,H	8F	ADC A	BA	CMP D	E5	PUSH H
0F	RRC	3A	LDA Adr	65	MOV H,L	8G	SUB B	BB	CMP E	E6	ANI D8
10	– –	3B	DCX SP	66	MOV H,M	91	SUB C	BC	CMP H	E7	RST 4
11	LXI D,D16	3C	INR A	67	MOV H,A	92	SUB D	BD	CMP L	E8	RPE
12	STAX D	3D	DCR A	68	MOV L,B	93	SUB E	BE	CMP M	E9	PCHL
13	INX D	3E	MVI A,D8	69	MOV L,C	94	SUB H	BF	CMP A	EA	JPE Adr
14	INR D	3F	CMC	6A	MOV L,D	95	SUB L	C0	RNZ	EB	XCHG
15	DCR D	40	MOV B,B	6B	MOV L,E	96	SUB M	C1	POP B	EC	CPE Adr
16	MVI D,D8	41	MOV B,C	6C	MOV L,H	97	SUB A	C2	JNZ Adr	ED	– –
17	RAL	42	MOV B,D	6D	MOV L,L	98	SBB B	C3	JMP Adr	EE	ERI D8
18	– –	43	MOV B,E	6E	MOV L,M	99	SBB C	C4	CNZ Adr	EF	RST 5
19	DAD D	44	MOV B,H	6F	MOV L,A	9A	SBB D	C5	PUSH B	F0	RP
1A	LDAX D	45	MOV B,L	70	MOV M,B	9B	SBB E	C6	ADI D8	F1	POP PSW
1B	DCX D	46	MOV B,M	71	MOV M,C	9C	SBB H	C7	RST 0	F2	JP Adr
1C	INR E	47	MOV B,A	72	MOV M,D	9D	SBB L	C8	RZ	F3	DI
1D	DRC E	48	MOV C,B	73	MOV M,E	9E	SBB M	C9	RET Adr	F4	CP Adr
1E	MVI E,D8	49	MOV C,C	74	MOV M,H	9F	SBB A	CA	JZ	F5	PUSH PSW
1F	RAR	4A	MOV C,D	75	MOV M,L	A0	ANA B	CB	– –	F6	ORI D8
20	RIM	4B	MOV C,E	76	HLT	A1	ANA C	CC	CZ Adr	F7	RST 6
21	LXI H,D16	4C	MOV C,H	77	MOV M,A	A2	ANA D	CD	CALL Adr	F8	RM
22	SHLD Adr	4D	MOV C,L	78	MOV A,B	A3	ANA E	CE	ACI D8	F9	SPHL
23	INX H	4E	MOV C,M	79	MOV A,C	A4	ANA H	CF	RST 1	FA	JM Adr
24	INR H	4F	MOV C,A	7A	MOV A,D	A5	ANA L	D0	RNC	FB	EI
25	DCR H	50	MOV D,B	7B	MOV A,E	A6	ANA M	D1	POP D	FC	CM Adr
26	MVI H,D8	51	MOV D,C	7C	MOV A,H	A7	ANA A	D2	JNC Adr	FD	– –
27	DAA	52	MOV D,D	7D	MOV A,L	A8	XRA B	D3	OUT D8	FE	CPI D8
28	– –	53	MOV D,E	7E	MOV A,M	A9	XRA C	D4	CNC Adr	FF	RST 7
29	DAD H	54	MOV D,H	7F	MOV A,A	AA	XRA D	D5	PUSH D		
2A	LHLD Adr	55	MOV D,L	80	ADD B	AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity. D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. Adr = 16-bit address.

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